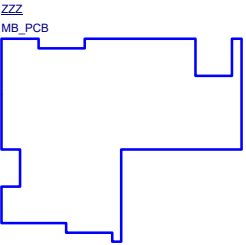


MODEL NAME : *APRDDB2000*
PCB NO : *LA-G661P*
BOM P/N : *431ADH31L0**



Dell/Compal Confidential

Schematic Document

Augusta Whiskey Lake U

BOM Structure

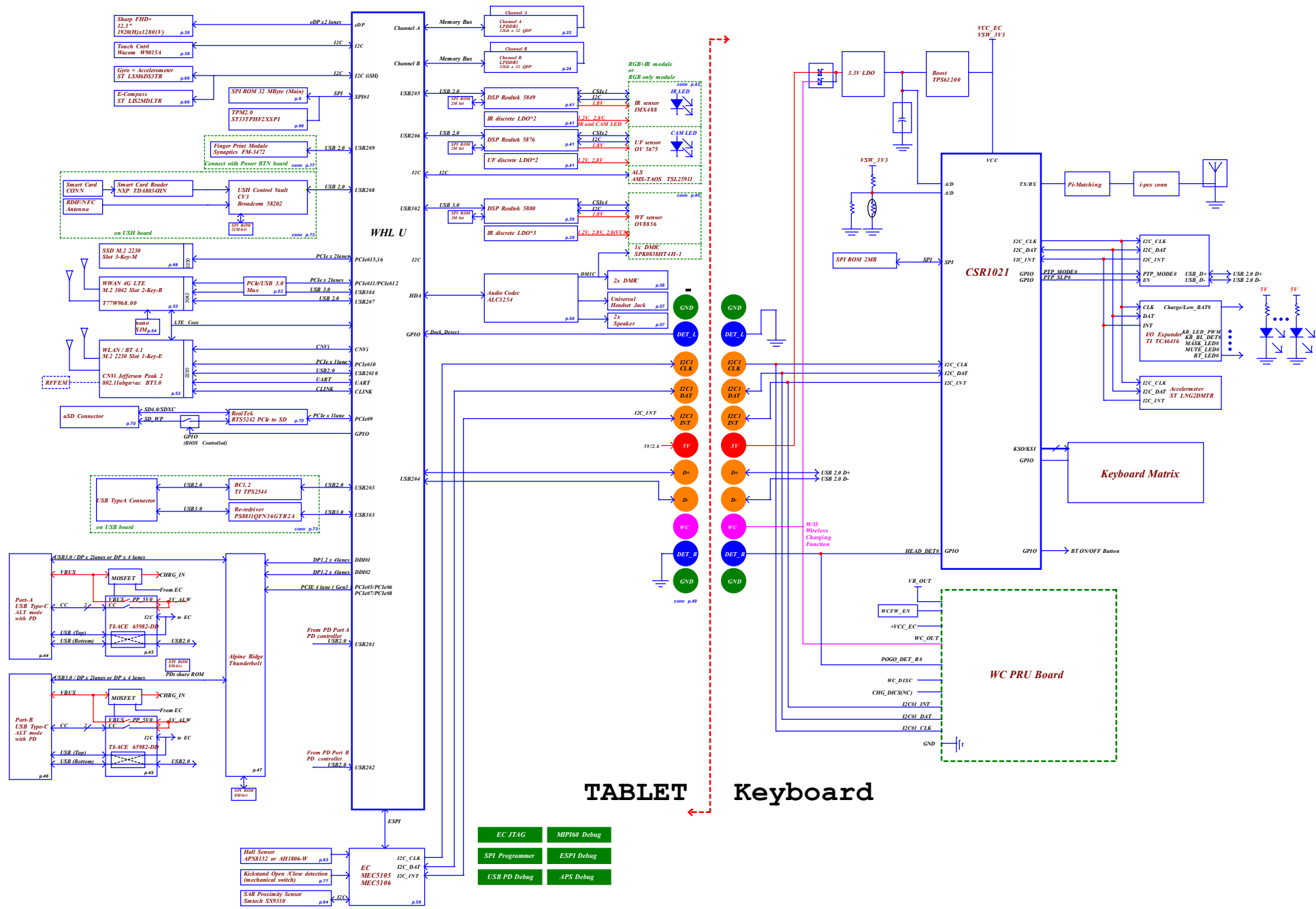
@ : Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
EMC@ : EMI Component
@EMC@ : EMI Nopop Component
ST@ : ST TPM
750@ : Nuvoton TPM
NRTD3@ : non RTD3 support
RTD3@ : RTD3 support
XDP@ : XDP Component
DB@ : Debug Component
BreakDown@ : Breakdown Component
U22@ : CPU U22 identify for BIOS
U42@ : CPU U42 identify for BIOS
U22EC@ : CPU U22 identify for EC
U42EC@ : CPU U42 identify for EC
5105@ : Option for MEC5105
5106@ : Option for MEC5106

NDS3@ : non Deep sleep Support
DS@ : Support Deep sleep
CPUI7@ : I7 CPU identify for BIOS
CPUI5@ : I5 CPU identify for BIOS
CPUI7EC@ : I7 CPU identify for EC
CPUI5EC@ : I5 CPU identify for EC
TPS79801QDGNR@ : Camera sensor AVDD main LDO
TPS7A1601DGNR@ : Camera sensor AVDD 2nd LDO
GIGADEVICE@ : BIOS ROM Option
WINBOND@ : BIOS ROM Option
MXIC@ : BIOS ROM Option

2019-03-05

Rev: 0.4 (X03)
PVT

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			Size	Document Number
			Date	Rev
			Tuesday, March 05, 2019	04
			Sheet	1 of 100



Vcc	3.3V +/- 5%		
Board ID	R	C	REV
0	240K +/- 5%	4700p	EXT1
1	130K +/- 5%	4700p	DVT1
2	62K +/- 5%	4700p	DVT2
3	33K +/- 5%	4700p	PVT
4	8.2K +/- 5%	4700p	
5	4.3K +/- 5%	4700p	
6	2K +/- 5%	4700p	
7	NC		

USB 2.0 PORT#	DESTINATION
1	TBT1
2	TBT2
3	USB Type-A
4	Dock
5	IR Camera
6	UF Camera
7	WWAN
8	USH
9	FPR
10	BT

DDI	DDI PORT#	DESTINATION
	1	TBT Alpine Ridge
	2	
eDP	1	FHD

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	1.0
6	
7	

@ : means de-pop

 : means Digital Ground

 : means Analog Ground

Flexible I/O	Interface	DESTINATION
1	PCI-E#1 / USB 3.0#1	
2	PCI-E#2 / USB 3.0#2	WF Camera
3	PCI-E#3 / USB 3.0#3	USB3.0 Type-A
4	PCI-E#4 / USB 3.0#4	NGFF (WWAN)
5	PCI-E#5 / USB 3.0#5	TBT Alpine Ridge
6	PCI-E#6 / USB 3.0#6	
7	PCI-E #7	
8	PCI-E #8	
9	PCI-E #9	Card reader
10	PCI-E #10	WLAN PCIe Gen2
11	PCI-E #11 /SATA #0	WWAN (2nd SSD)
12	PCI-E #12 /SATA #1A	
13	PCI-E #13	
14	PCI-E #14	
15	PCI-E #15 /SATA #1B	Main SSD (2230)
16	PCI-E #16 /SATA #2	

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	TBT AR
	CLKOUT_PCIE1	Main SSD
	CLKOUT_PCIE2	WWAN (2nd SSD)
	CLKOUT_PCIE3	WLAN PCIe Gen2
	CLKOUT_PCIE4	Card Reader
	CLKOUT_PCIE5	N/A

[illegible]

The diagram illustrates the hardware configuration of the AWS Graviton2 instance, showing the CPU Option, VMT2_2, VMT2_1, PVT, and EC Option configurations.

CPU Option: The CPU Option is configured with 16 vCPUs and 64 GB of memory. The configuration includes 16 vCPUs (Graviton2) and 64 GB of memory (Graviton2).

VMT2_2: The VMT2_2 configuration includes 16 vCPUs (Graviton2) and 64 GB of memory (Graviton2). The configuration also includes 16 vCPUs (Graviton2) and 64 GB of memory (Graviton2).

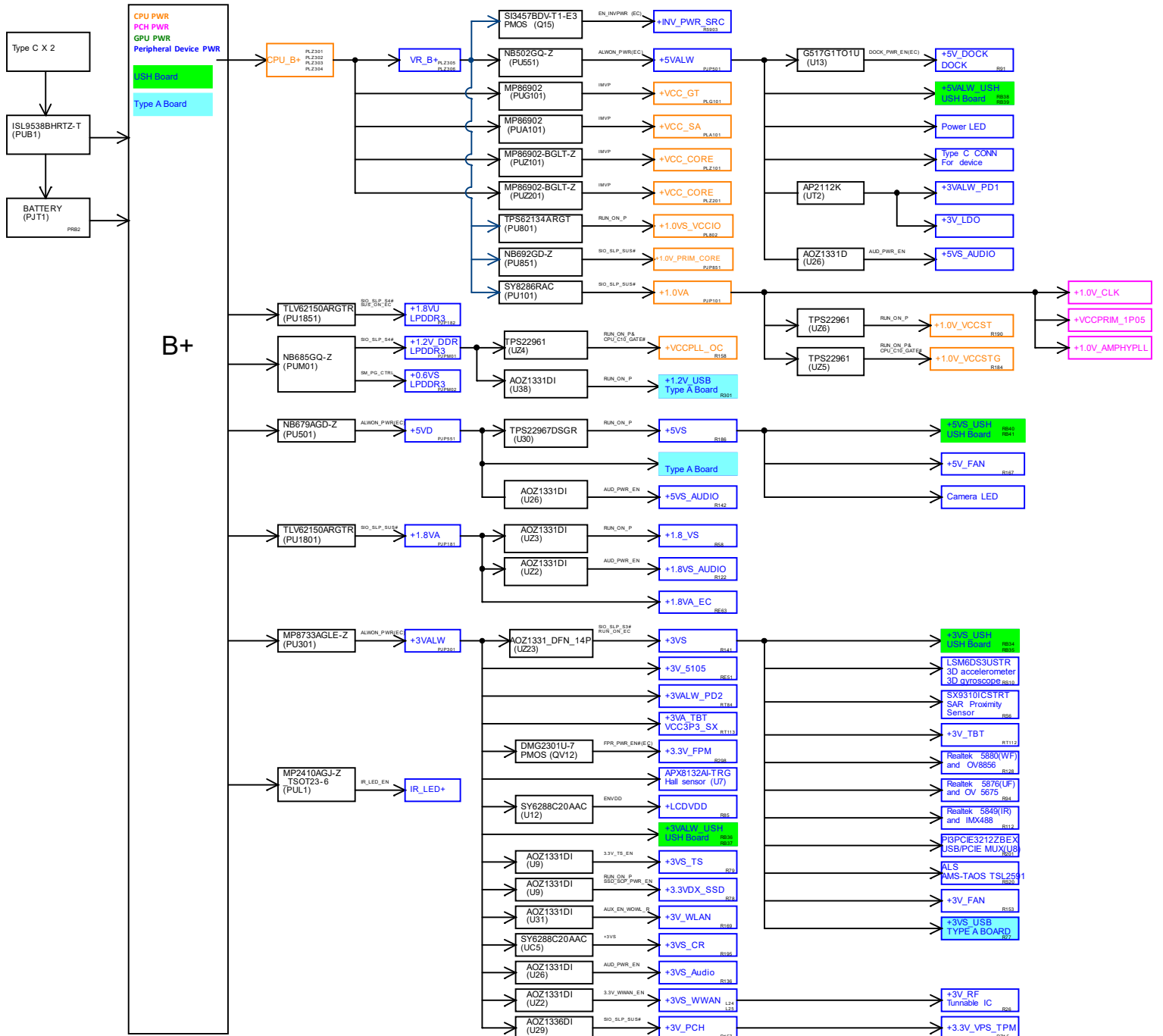
VMT2_1: The VMT2_1 configuration includes 16 vCPUs (Graviton2) and 64 GB of memory (Graviton2). The configuration also includes 16 vCPUs (Graviton2) and 64 GB of memory (Graviton2).

PVT: The PVT configuration includes 16 vCPUs (Graviton2) and 64 GB of memory (Graviton2). The configuration also includes 16 vCPUs (Graviton2) and 64 GB of memory (Graviton2).

EC Option: The EC Option is configured with 16 vCPUs and 64 GB of memory. The configuration includes 16 vCPUs (Graviton2) and 64 GB of memory (Graviton2).

Figure 6-17. High Speed I/O (HSIO) Lane Multiplexing in ICL U PCH-LP

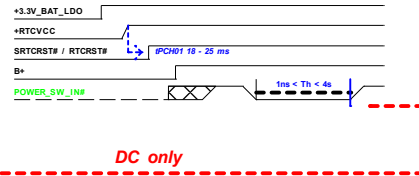
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	GbE	GbE	GbE		SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2
Intel® RST Support	No Support			No Support			Yes			Yes						



[AC in] (remove RTC)

[AC in] (remove RTC)

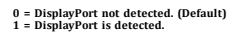
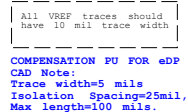
[Battery only, AC absent] (remove RTC)



DC only

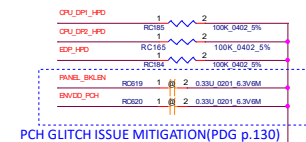
----- AC only

POWER_SW_IN# (AC only)

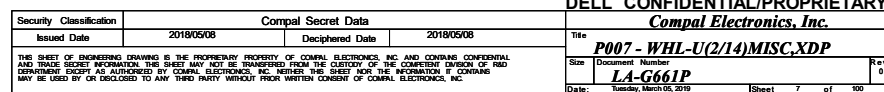
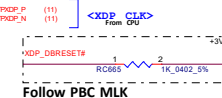
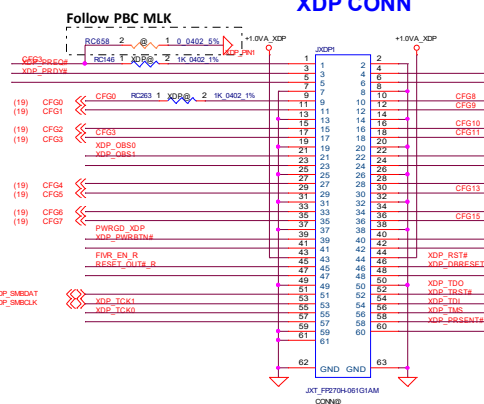
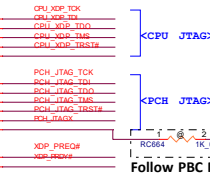
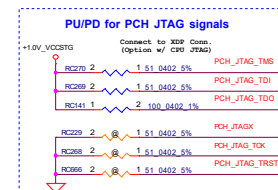


GPP_H17 (WEAK INTERNAL PD)

This signal has a weak internal pull-down.
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.



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Date: Monday, January 26, 2015			Sheet 6 of 100	



DEX_VTT_OVL

UC2A

1 NC

2 Y

3 A

4 GND

5 VCC

74VHC1G070W_TSSOP5

+1.2V_DDR

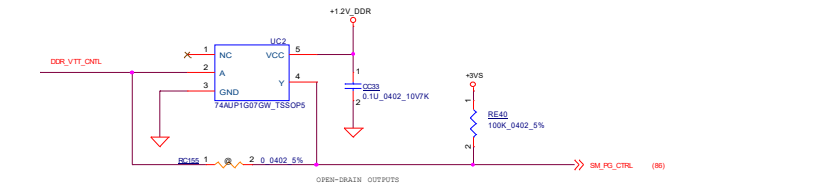
+3V3

RE40

100K_0402_5%

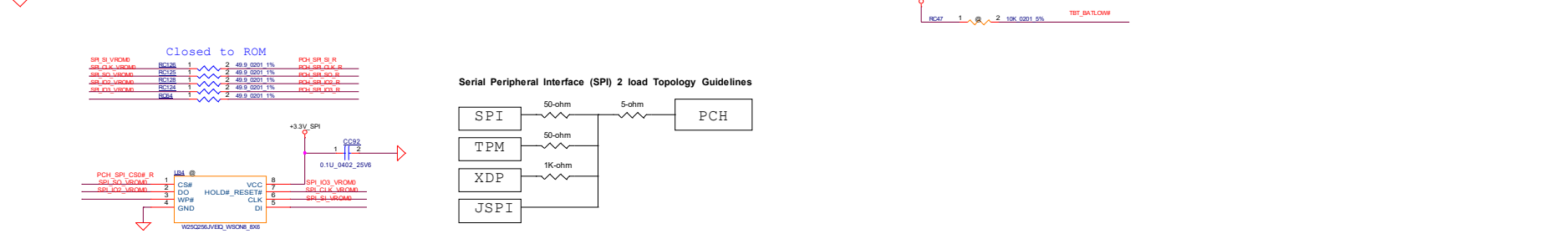
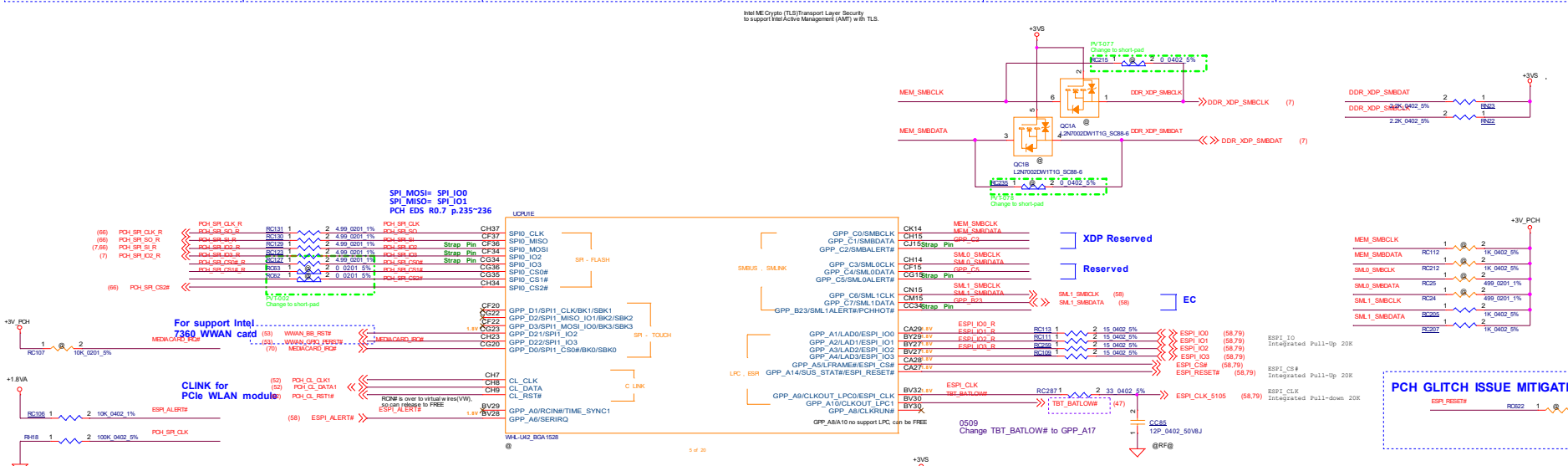
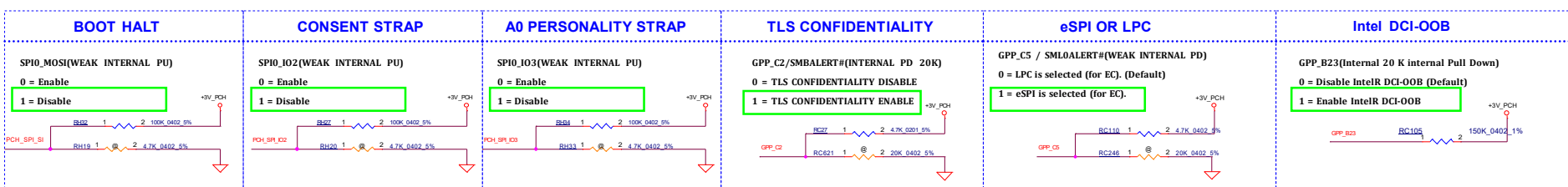
DEX_PO_CTL (NM)

OPEN-DRAIN OUTPUTS



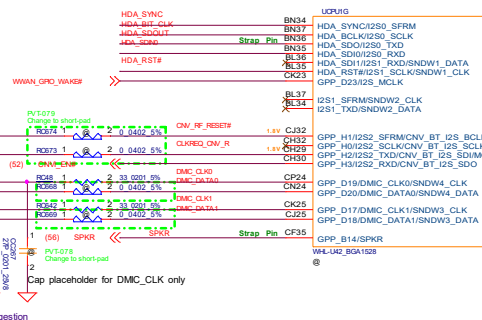
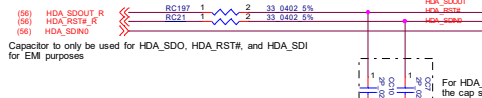
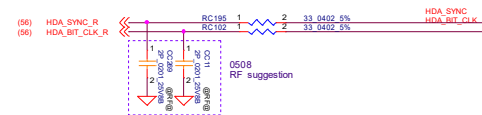
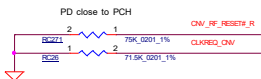
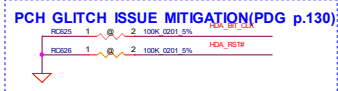
Jony12/14:572136_CFL_U_LP3_Memory_Design_Sch_WP_Rev0p5.pdf - Keep setting

CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

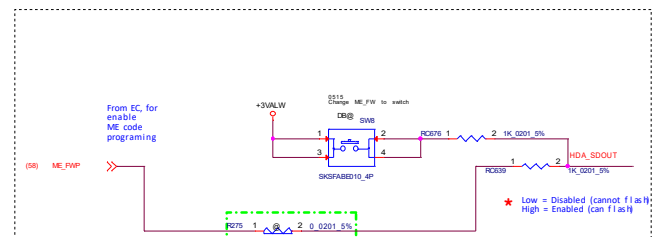
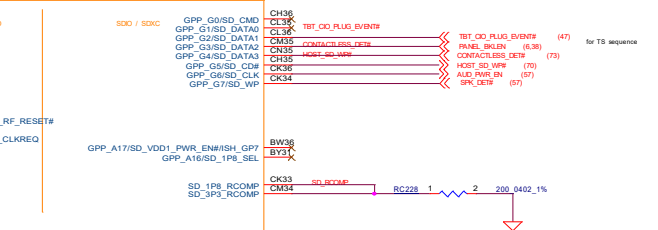
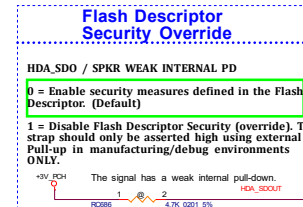
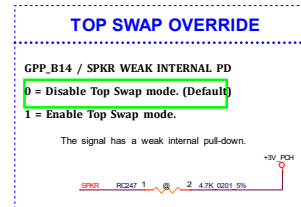
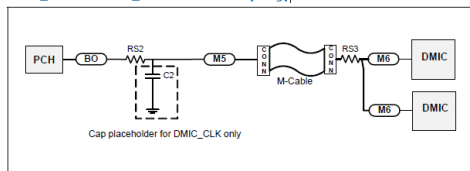


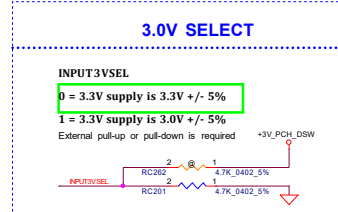
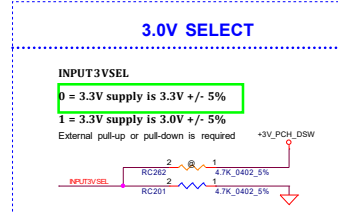
Serial Peripheral Interface (SPI) 2 load Topology Guidelines					
SPI	50-ohm	5-ohm	PCH		
TPM	50-ohm				
XDP	1K-ohm				
JSPI					

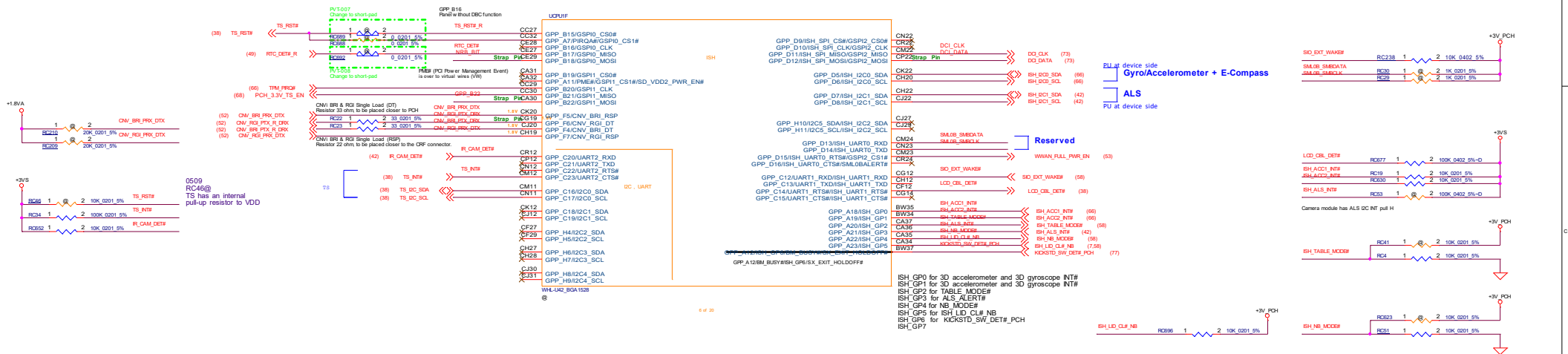
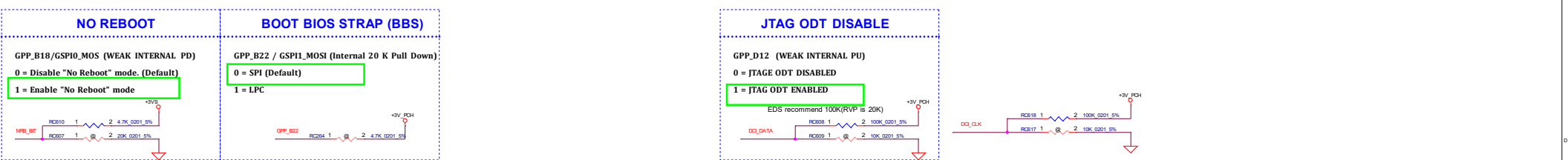
CPU	EC chipset	EC code	BIOS code	BIOS ROM source	BIOS File name
QS consumer	5105	Legacy	code 5	GIGADEVICE SA0000BGM00	AUG020_QS_5105_L.bin
QS consumer	5105	RTOS	code 3	WINBOND SA00009RI10	AUG020_QS_5105_R.bin
QS consumer	5106	RTOS	code 4	WINBOND SA00009RI10	AUG020_QS_5106_R.bin
ES corp.	5105	RTOS	code 1	WINBOND SA00009RI10	AUG020_ES_5105_R.bin
ES corp.	5106	RTOS	code 2	MXIC SA0000BCD00	AUG020_ES_5106_R.bin



DMIC_CLK and DMIC_DATA Branched Topology







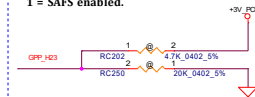
Camera module has ALS I2C RPT pull H

eSPI Flash Sharing Mode

GPP_H23 (WEAK INTERNAL PD)

0 = MAFS enabled (Default)

1 = SAFS enabled.



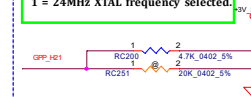
0 = Master Attached if as Sharing (MAFS) enabled. (Default)
1 = Slave Attached if as Sharing (SAFS) enabled.

XTAL Frequency Select

GPP_H21 (WEAK INTERNAL PD)

0 = 38.4 XTAL frequency selected. (Default)

1 = 24MHz XTAL frequency selected.



XTAL INPUT MODE (HVM ONLY)

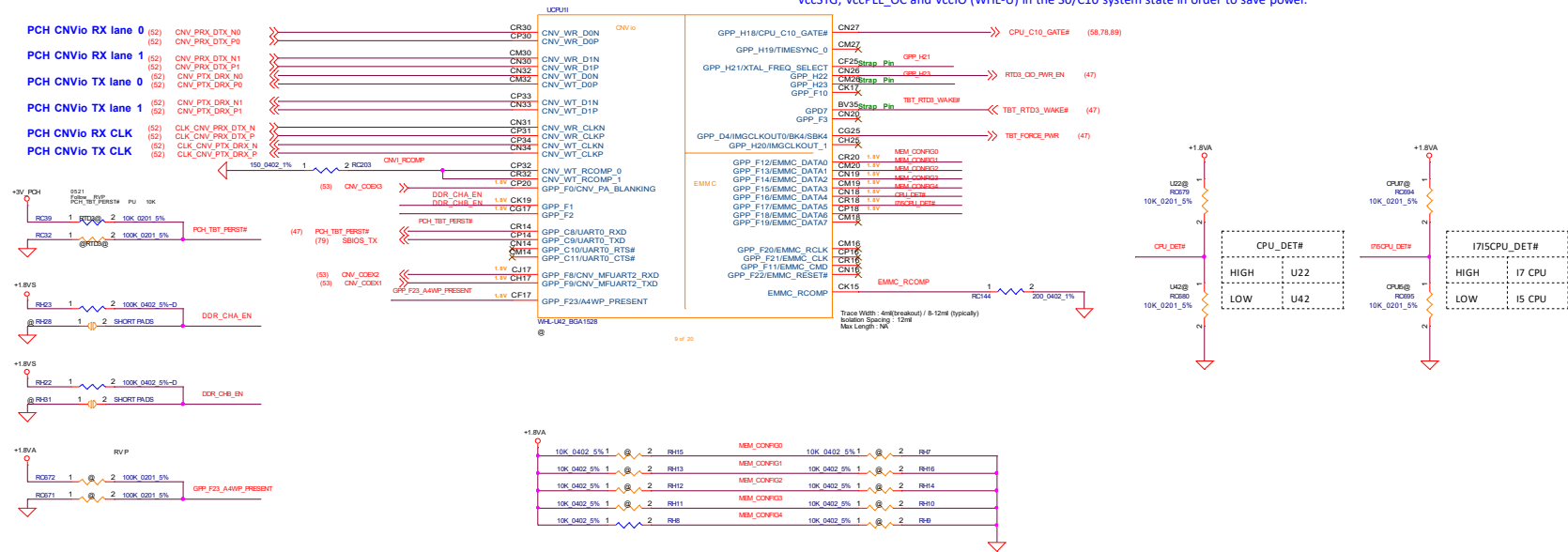
GPD7(External pull-up is required)

0 = XTAL INPUT IS SINGLE ENDED

1 = XTAL IS ATTACHED

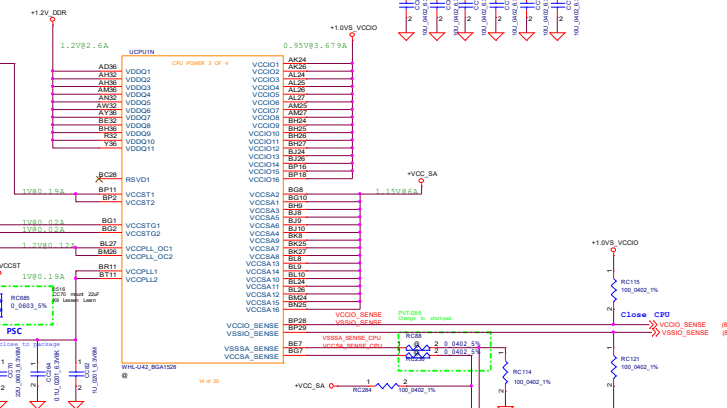


CPU_C10_GATE# is a new signal from the Whiskey Lake SoC that can be used for gate off VccSTG, VccPLL_OC and VccIO (WHL-U) in the S0/C10 system state in order to save power.

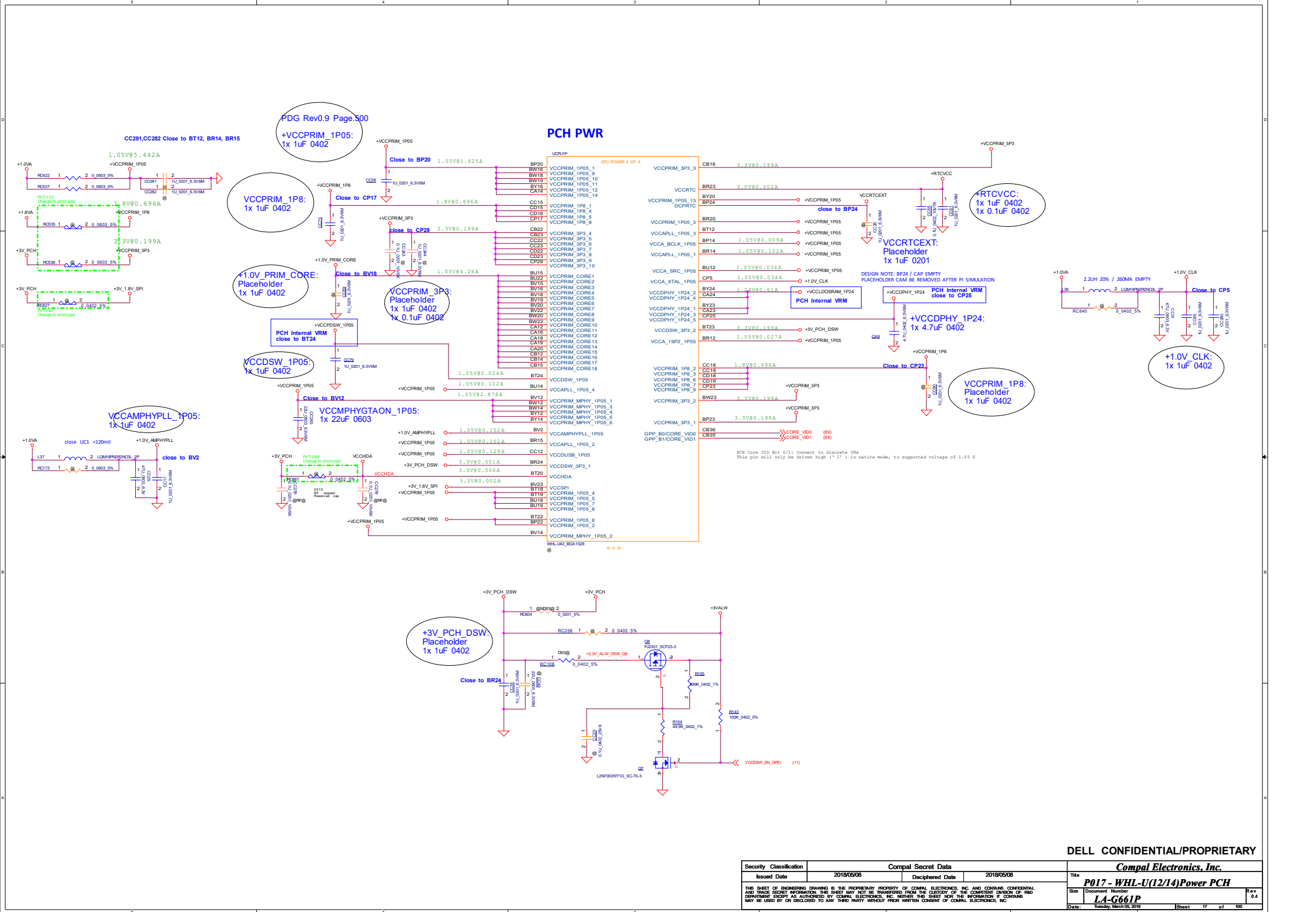


+VCC_G

1.5V@54A

[illegible]

Security Classification		Compal Secret Data		Compal Electronics, Inc. Title: P016 - WHL-U(11/14)Power GT,IO Size: LA-G661P Date: July 19, 2019		Rev: 0.0
Issued Date	2018/05/08	Deciphered Date	2018/05/08			
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				Drawn By: 7/19/2019		Sheet 16 of 18



Note1: VCCPRIM_CORE Implementation with PCH CORE_V D Recommendation

VCCPRIM_CORE		
CR34	VSS_1	BL7
B15	VSS_2	AE25
BY5	VSS_3	BM33
CP45	VSS_4	CM6
CM37	VSS_5	AE27
CK37	VSS_6	BM35
AW1	VSS_7	CM6
CM1	VSS_8	AE30
B06	VSS_9	BM35
AV4	VSS_10	CM13
B34	VSS_11	AE7
E35	VSS_12	BM9
AE4	VSS_13	CM17
AE26	VSS_14	BM30
AP25	VSS_15	CM21
AG24	VSS_16	BM3
AG26	VSS_17	CM7
AP25	VSS_18	CM25
AP25	VSS_19	CM25
AP25	VSS_20	CM25
AP25	VSS_21	CM25
AP25	VSS_22	CM25
AP25	VSS_23	CM25
AP25	VSS_24	CM25
AP25	VSS_25	CM25
AP25	VSS_26	CM25
AP25	VSS_27	CM25
AP25	VSS_28	CM25
AP25	VSS_29	CM25
AP25	VSS_30	CM25
AP25	VSS_31	CM25
AP25	VSS_32	CM25
AP25	VSS_33	CM25
AP25	VSS_34	CM25
AP25	VSS_35	CM25
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AP25	VSS_107	CM25
AP25	VSS_108	CM25
AP25	VSS_109	CM25
AP25	VSS_110	CM25
AP25	VSS_111	CM25
AP25	VSS_112	CM25
AP25	VSS_113	CM25
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AP25	VSS_115	CM25
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AP25	VSS_122	CM25
AP25	VSS_123	CM25
AP25	VSS_124	CM25
AP25	VSS_125	CM25
AP25	VSS_126	CM25
AP25	VSS_127	CM25
AP25	VSS_128	CM25
AP25	VSS_129	CM25
AP25	VSS_130	CM25
AP25	VSS_131	CM25
AP25	VSS_132	CM25
AP25	VSS_133	CM25
AP25	VSS_134	CM25
AP25	VSS_135	CM25
AP25	VSS_136	CM25
AP25	VSS_137	CM25
AP25	VSS_138	CM25
AP25	VSS_139	CM25
AP25	VSS_140	CM25
AP25	VSS_141	CM25
AP25	VSS_142	CM25
AP25	VSS_143	CM25
AP25	VSS_144	CM25

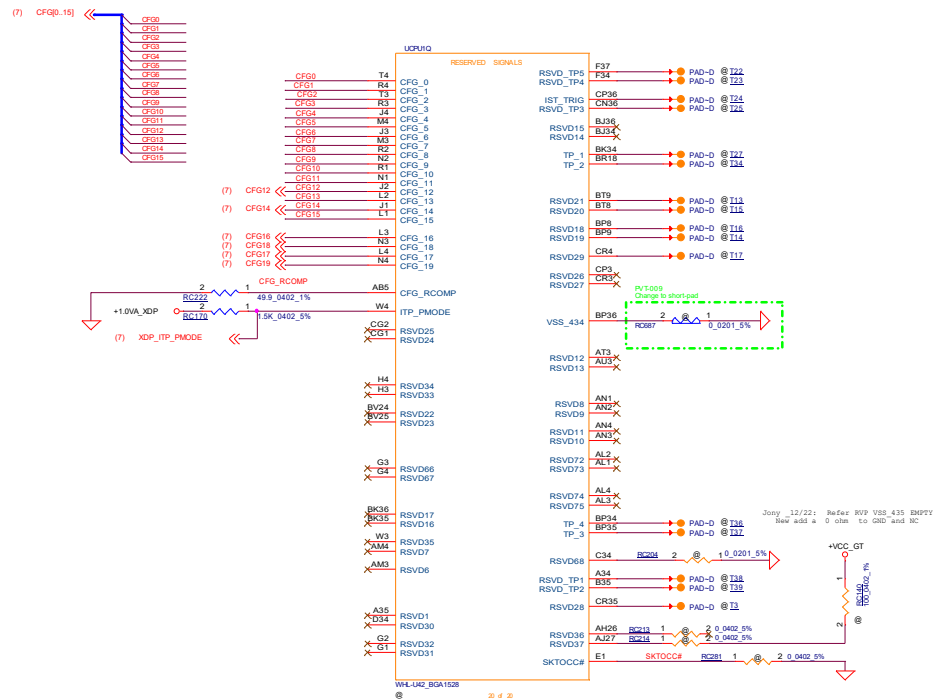
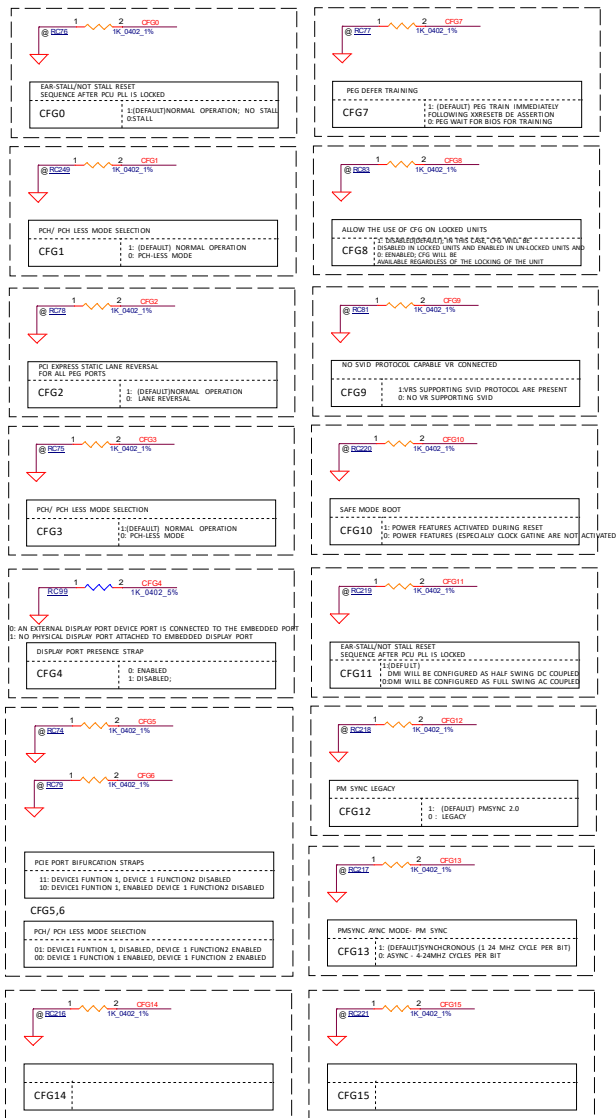
VCCPRIM_CORE		
BT35	VSS_145	AE25
DE	VSS_146	BM33
AE32	VSS_147	CM6
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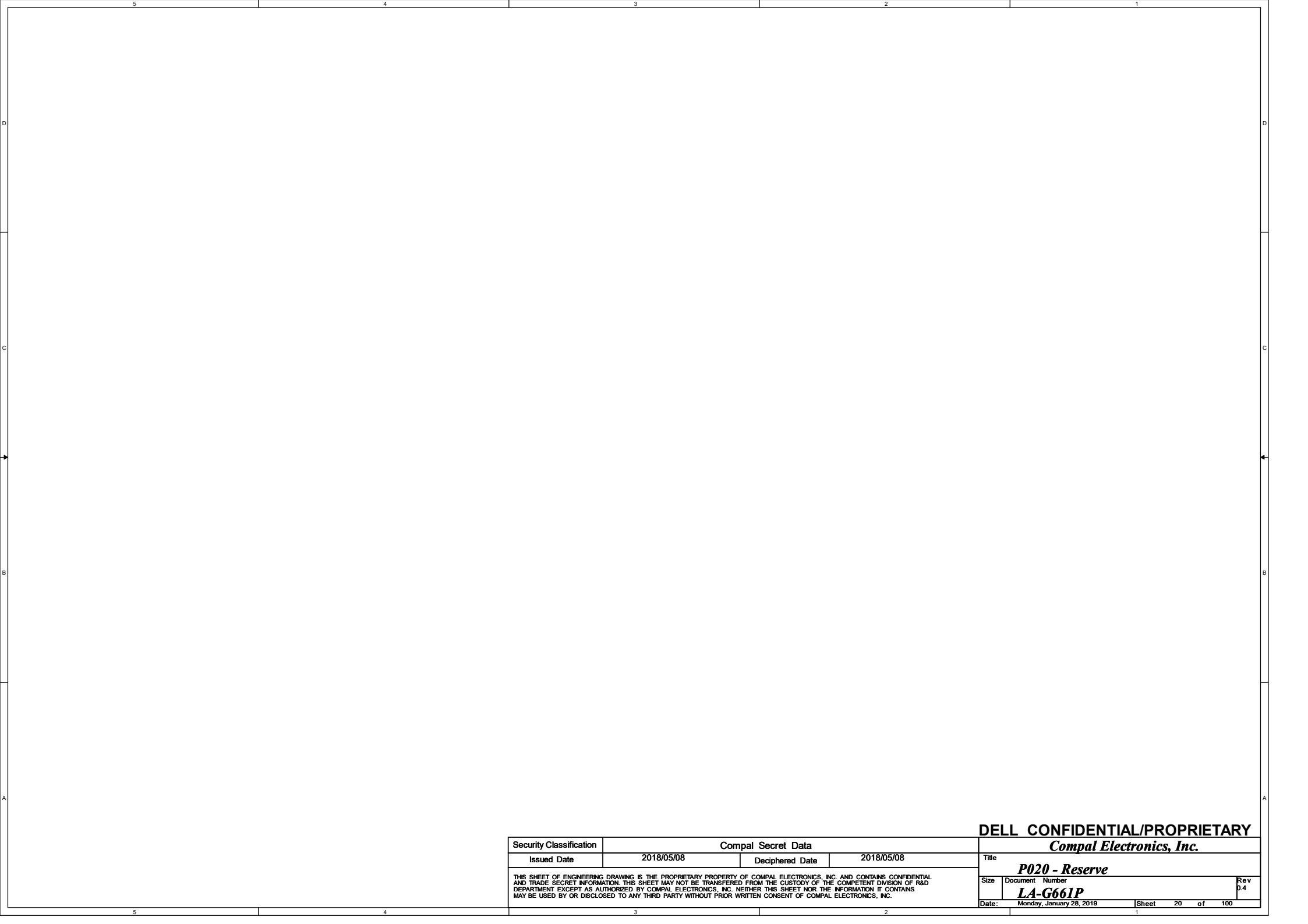
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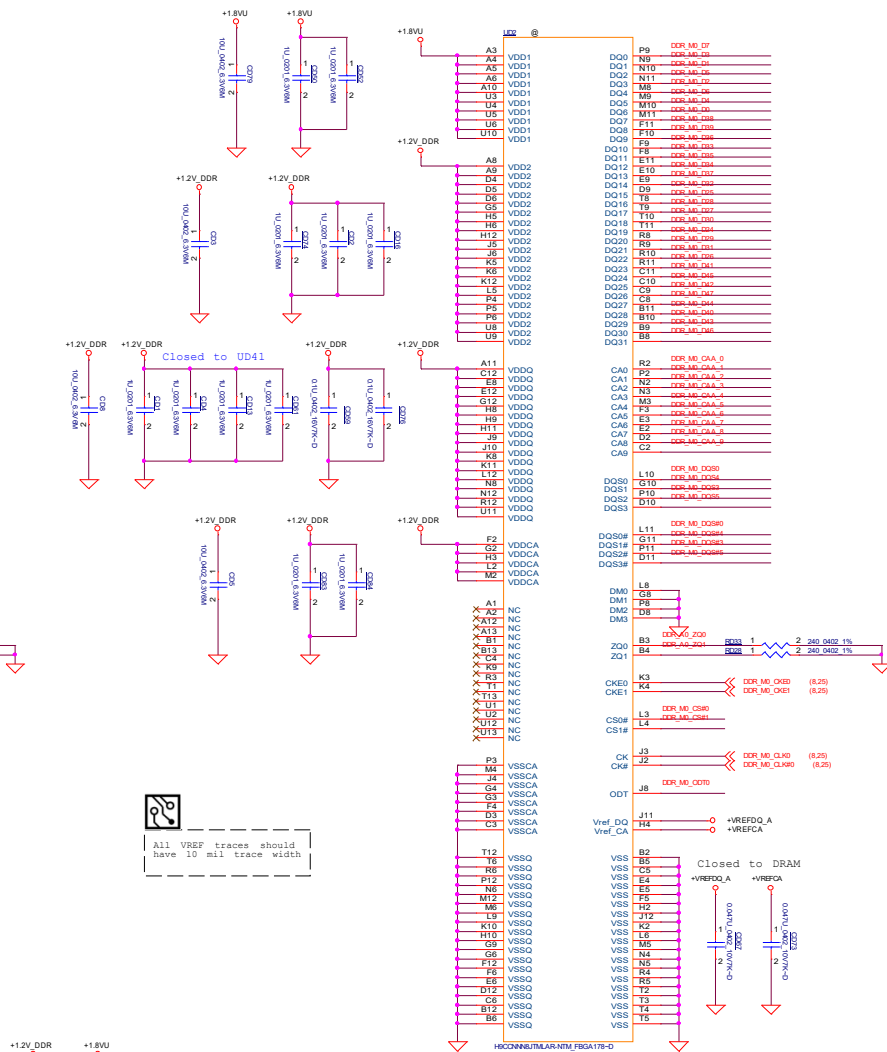
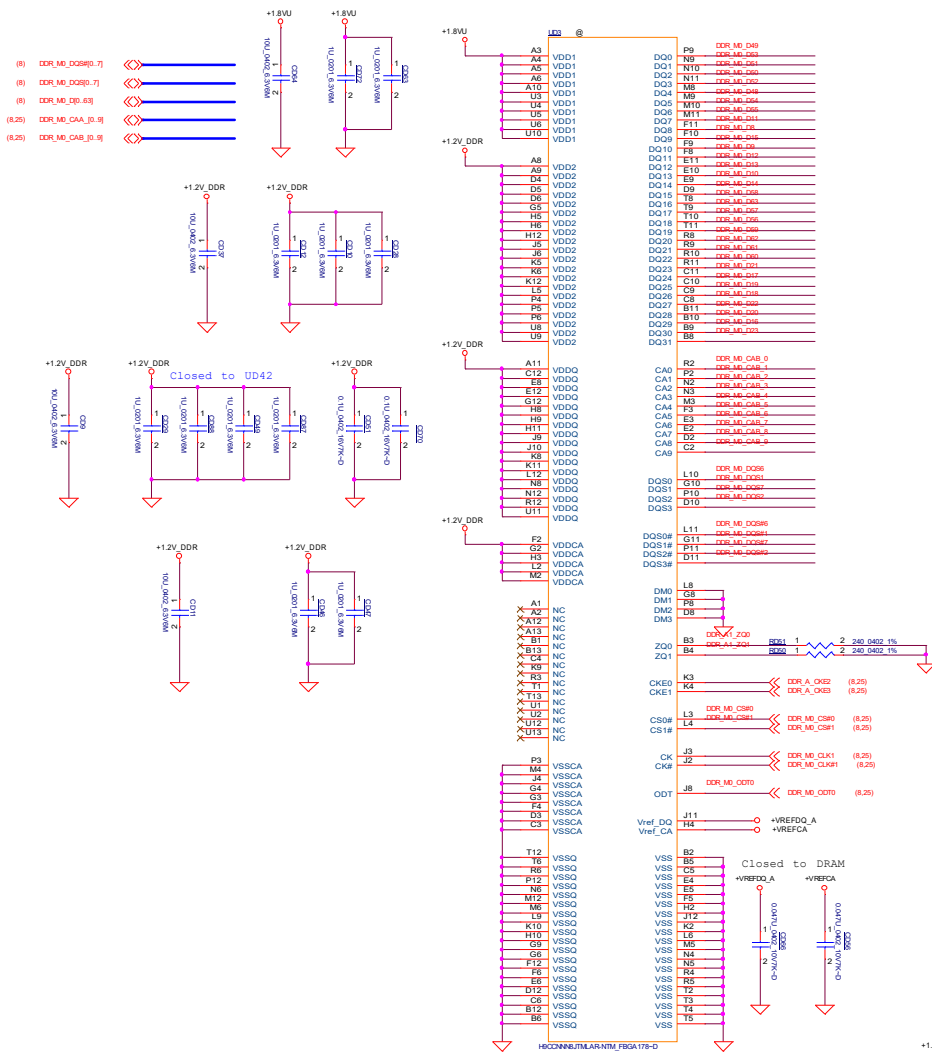


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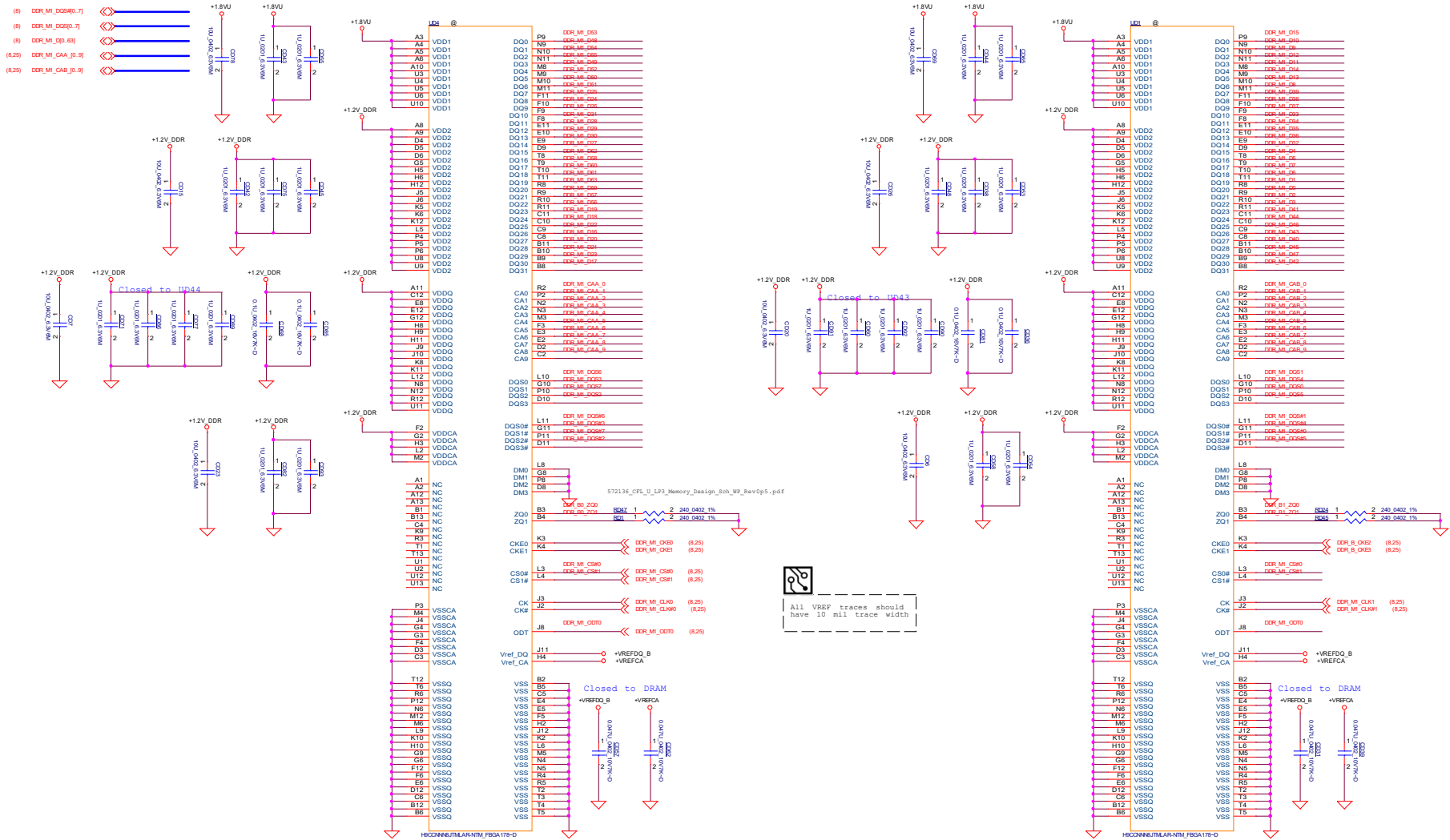
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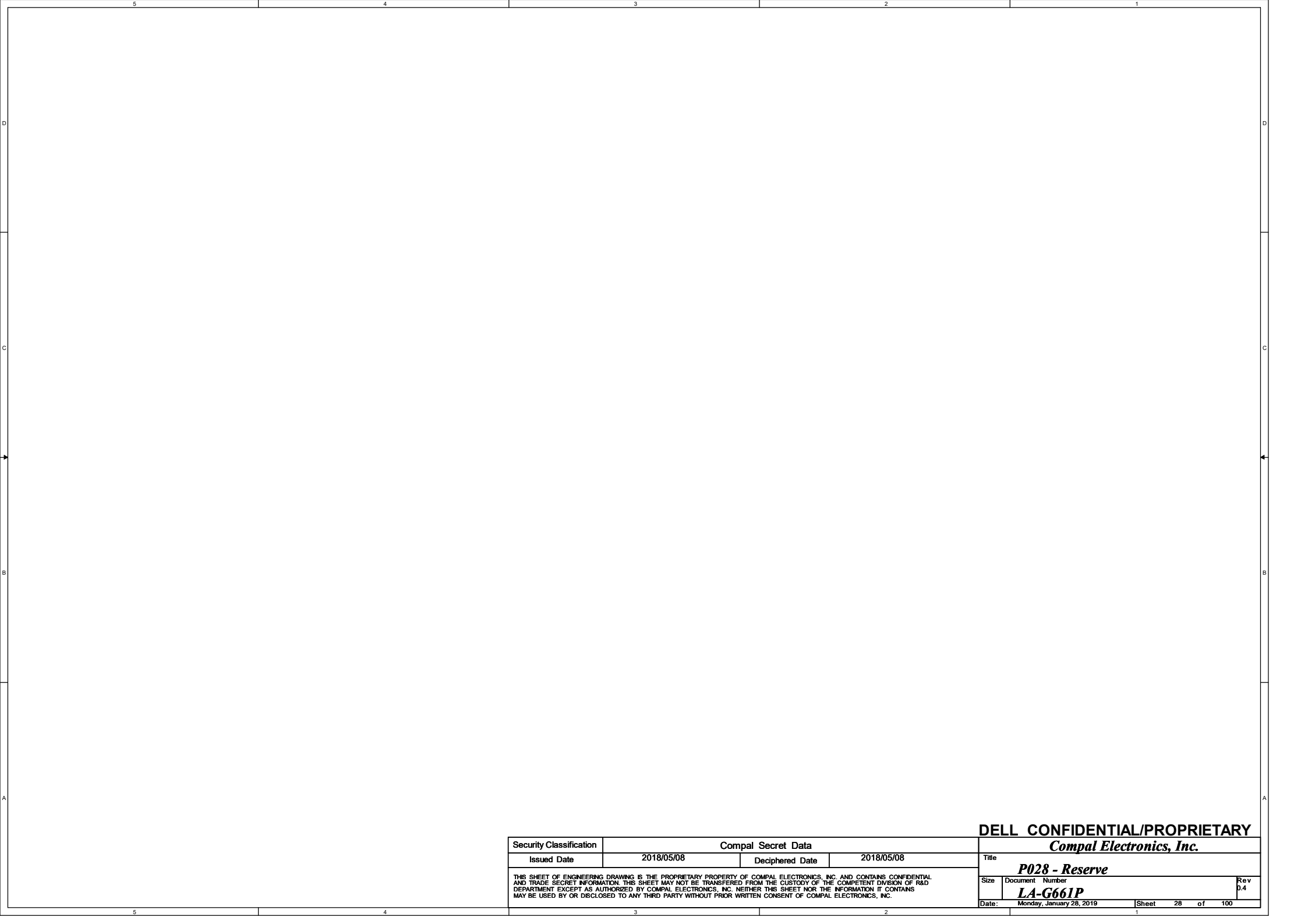
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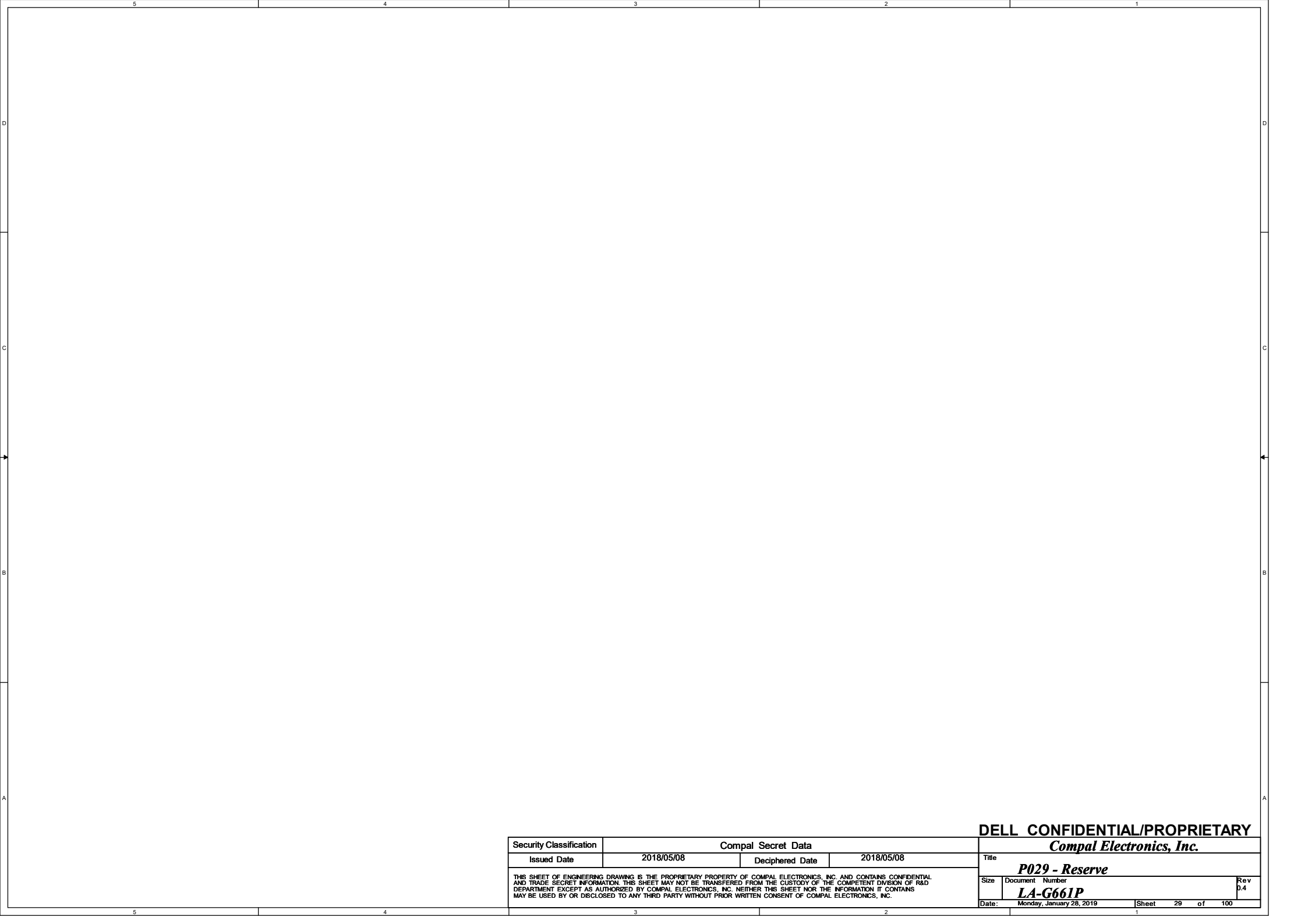
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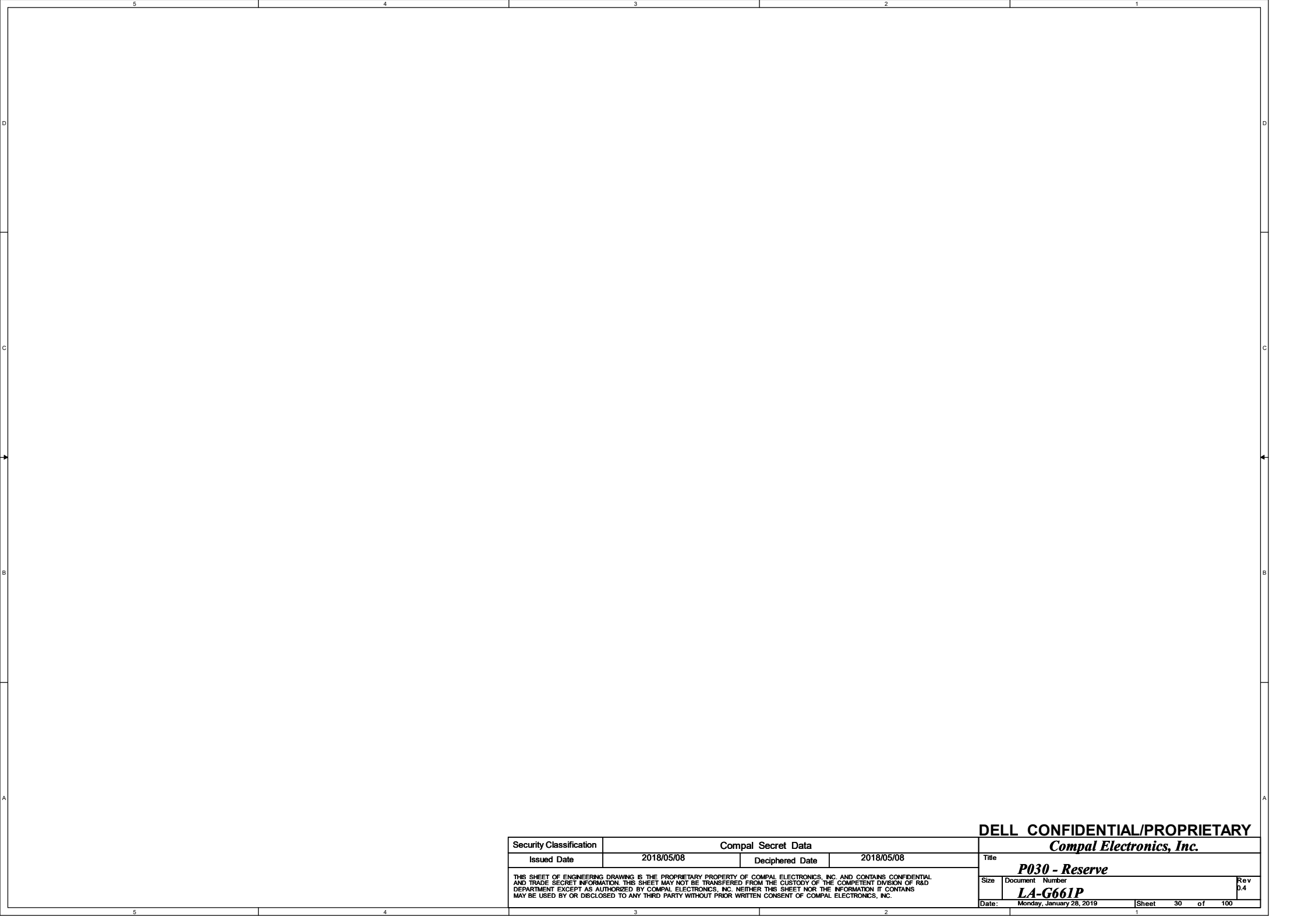


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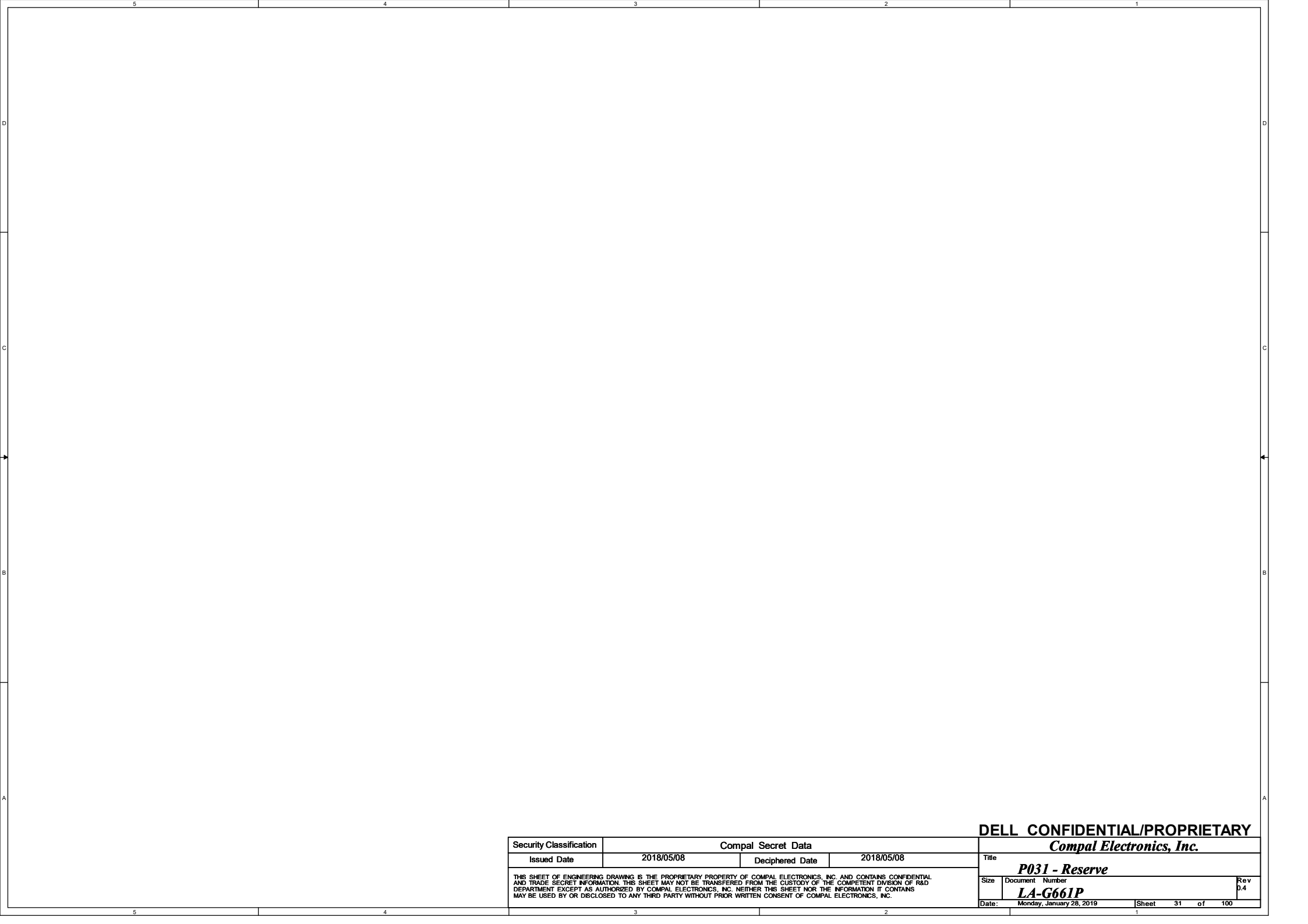
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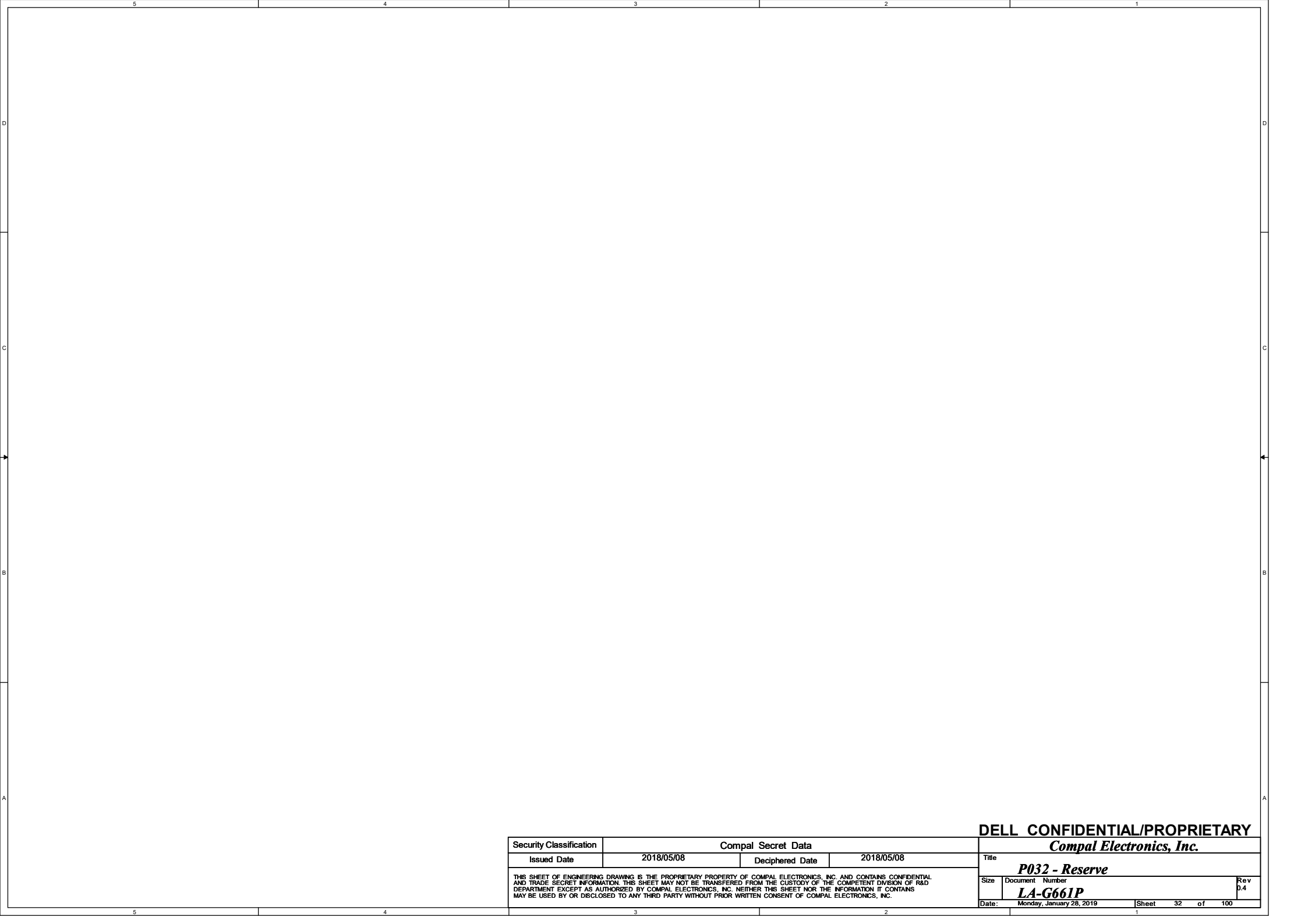
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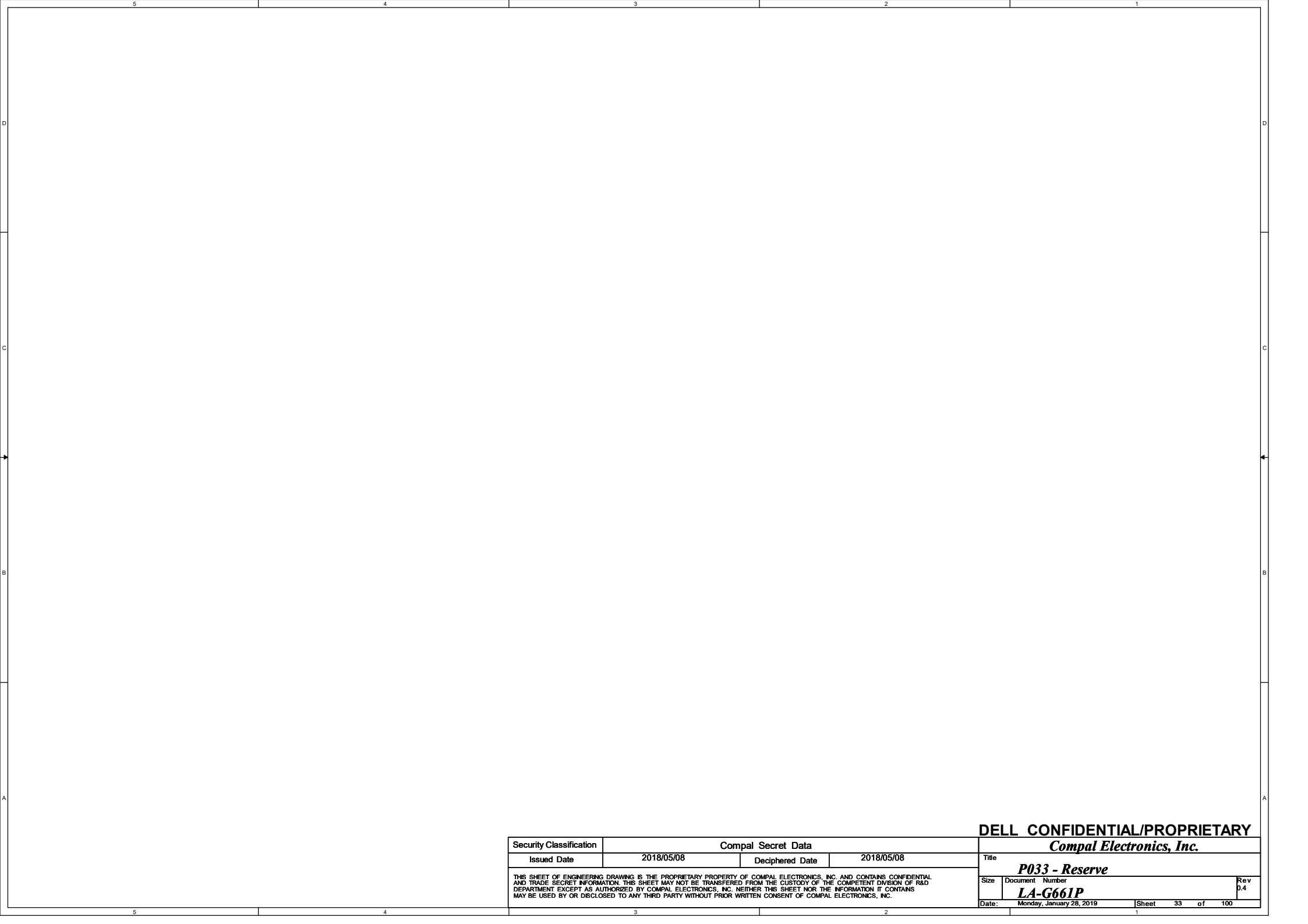
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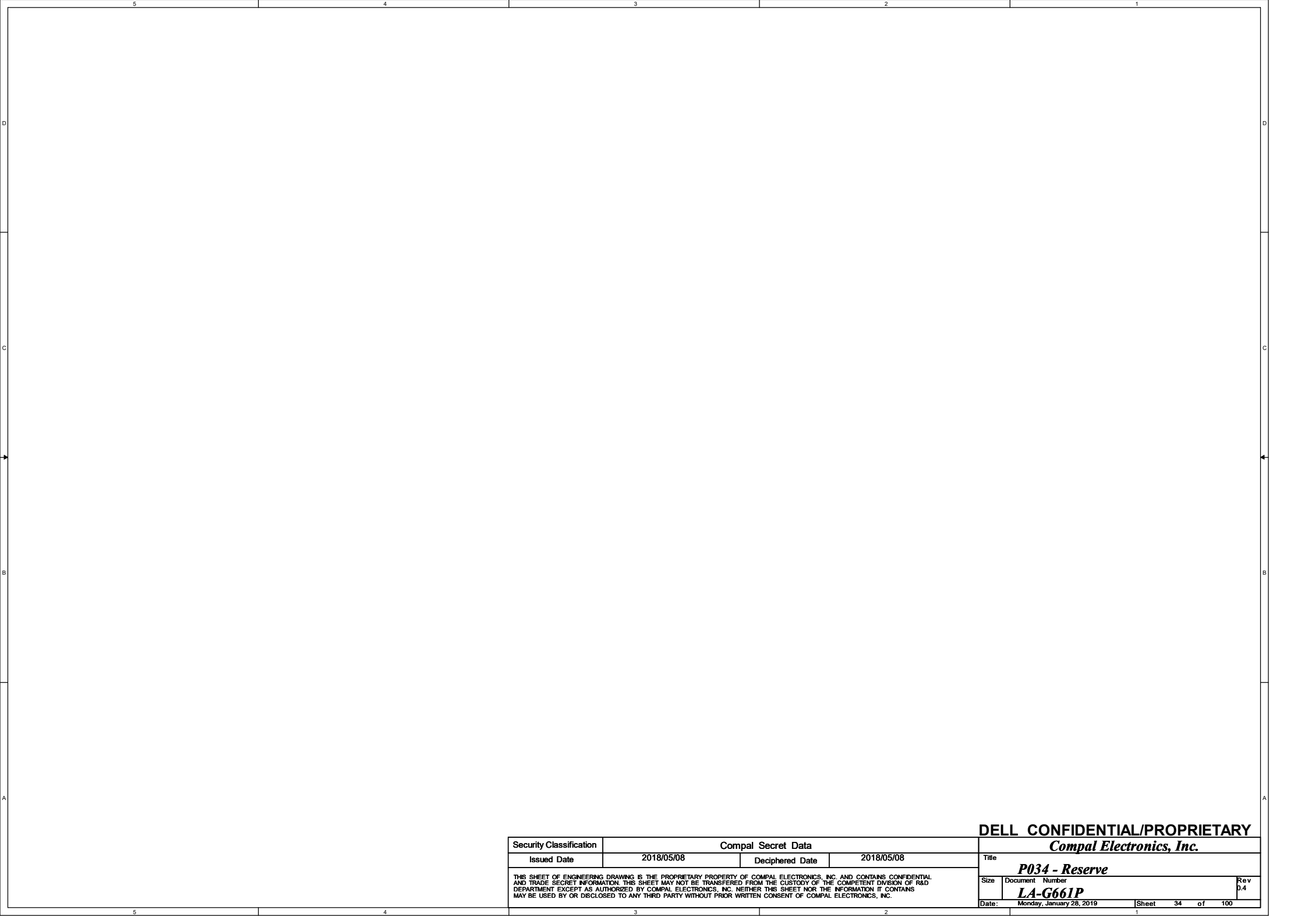
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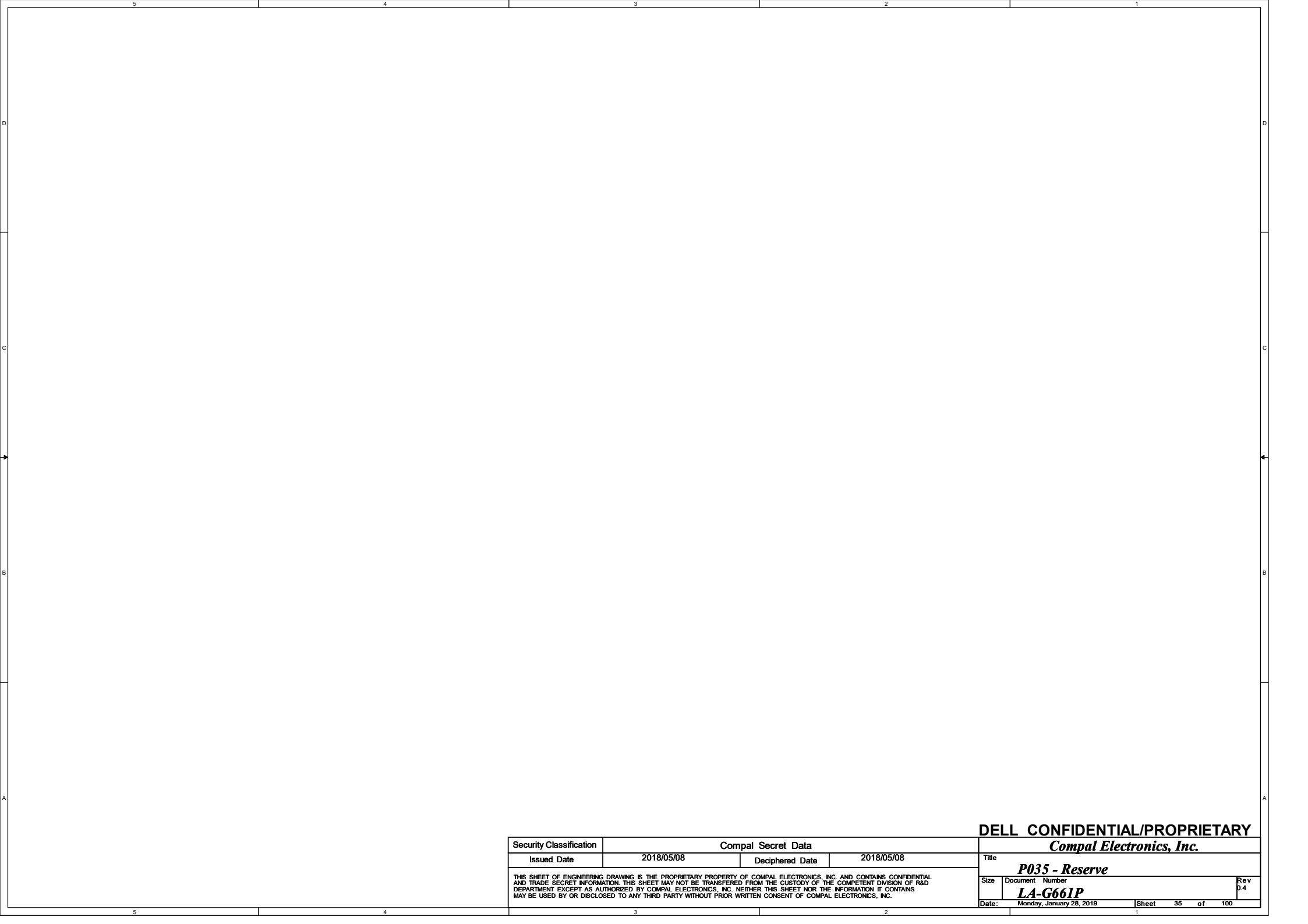
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				<i>LA-G661P</i>		
				Date:	Monday, January 28, 2019	Sheet 32 of 100



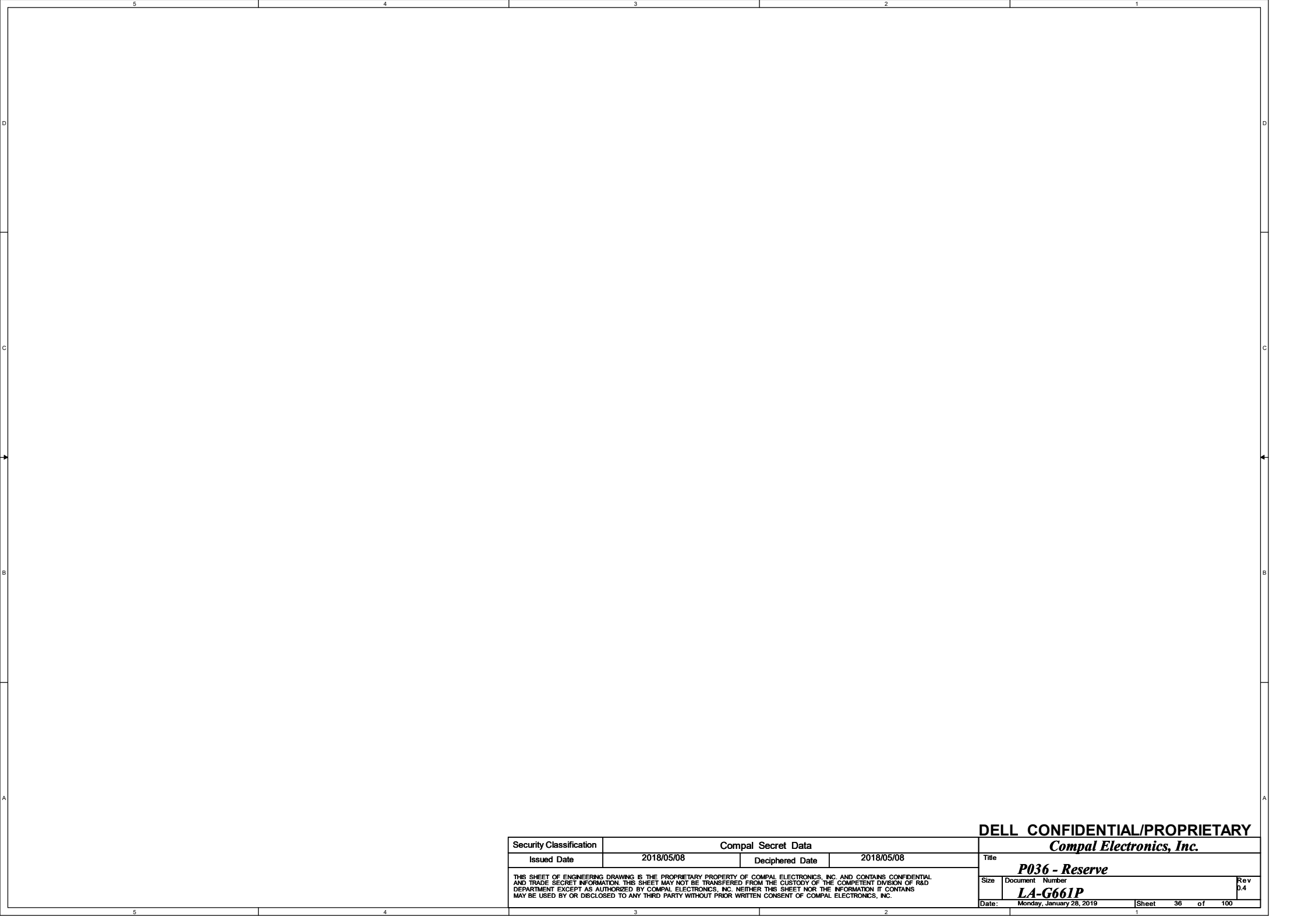
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					LA-G661P
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		Document Number			0.4
Date:		Monday, January 28, 2019		Sheet	35 of 100

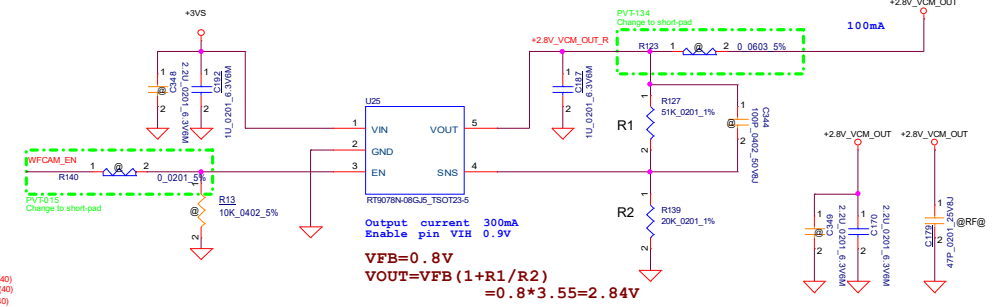


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				LA-G661P		
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		LA-G661P			0.4
Date:		Monday, January 28, 2019		Sheet	37 of 100

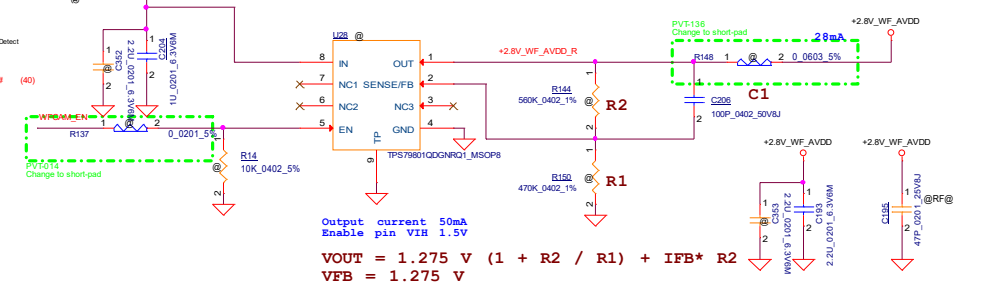
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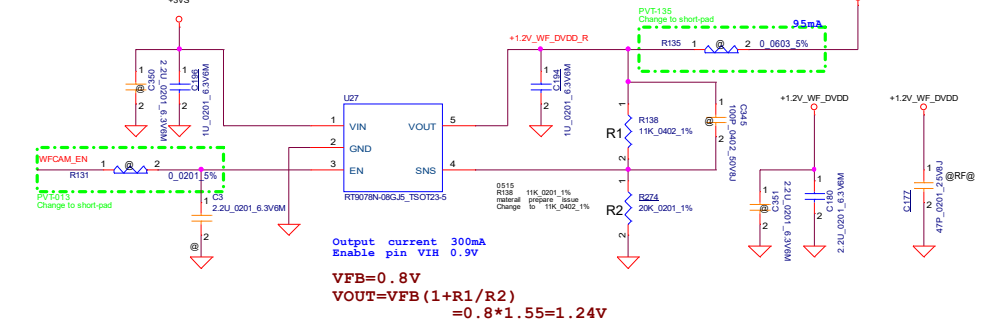
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U25	TPS79801QDGNR@ SA000040000	R1	470K
Vref=1.275 V			

LDO IC	TPS7A1601DGNR	R2	1.5M
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Vref=1.193V			

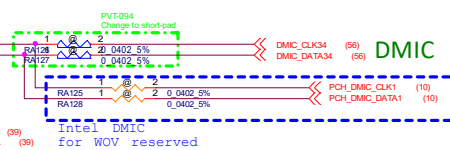
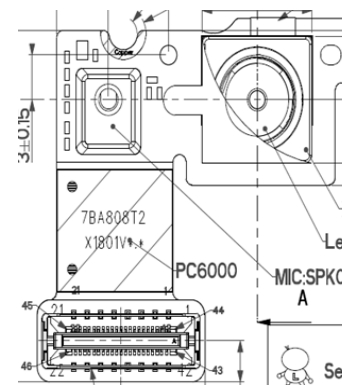
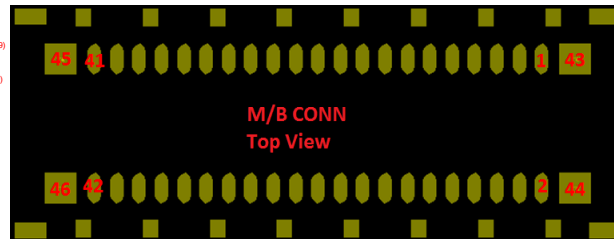
(+2.8V_WF_AVDD) For Rear Camera



(+1.2V_WF_DVDD) For Rear Camera

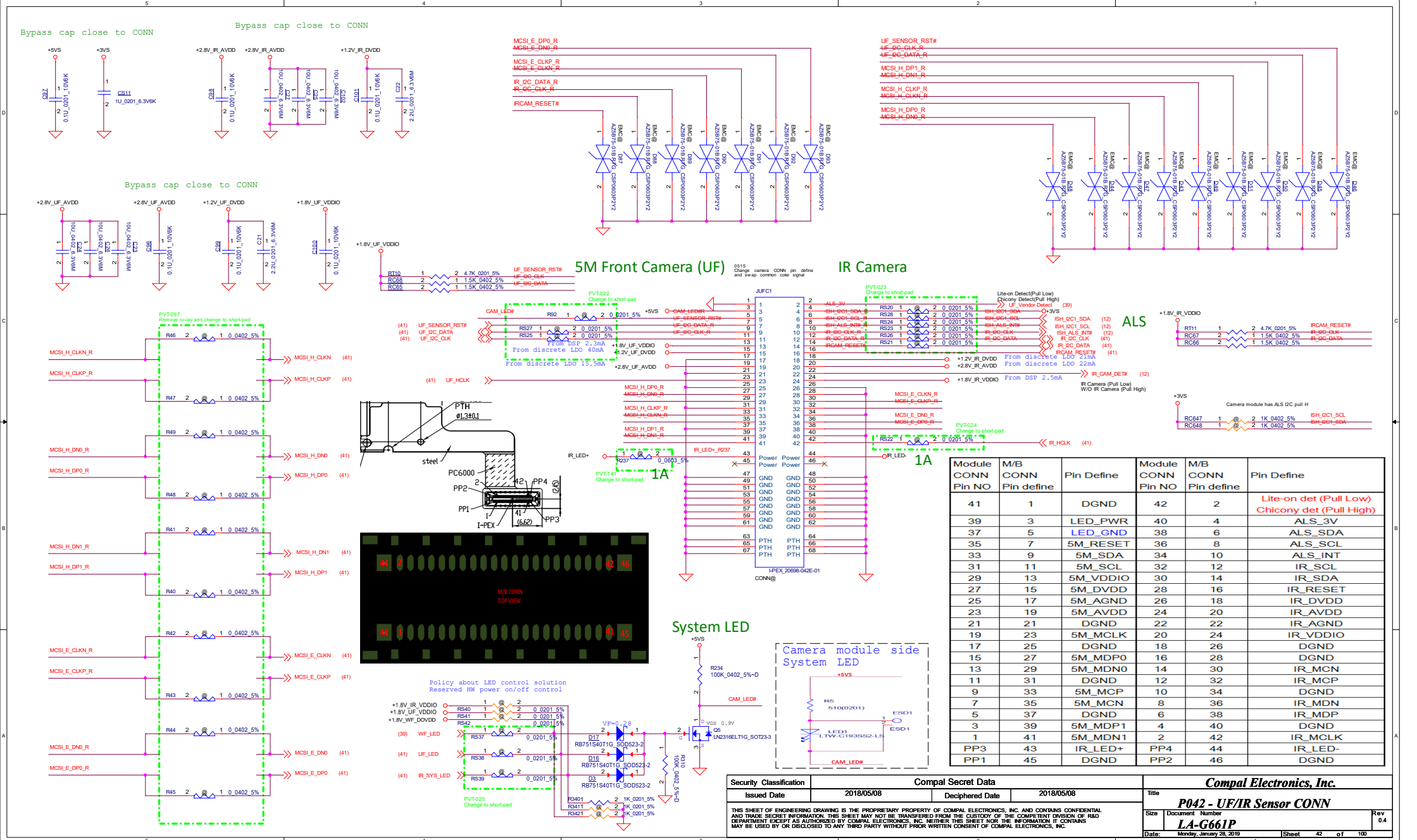


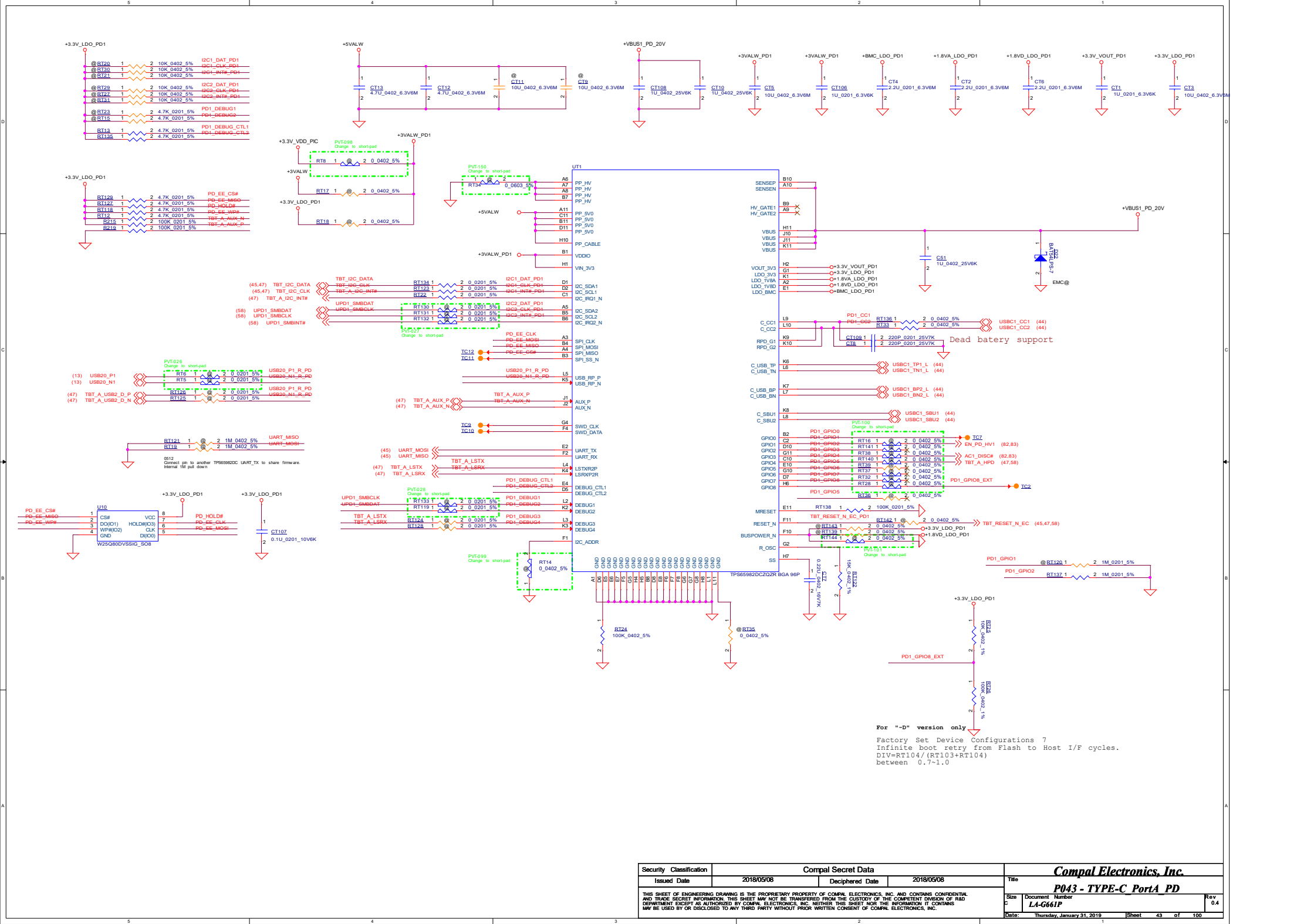
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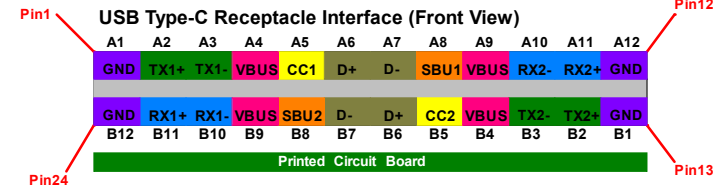
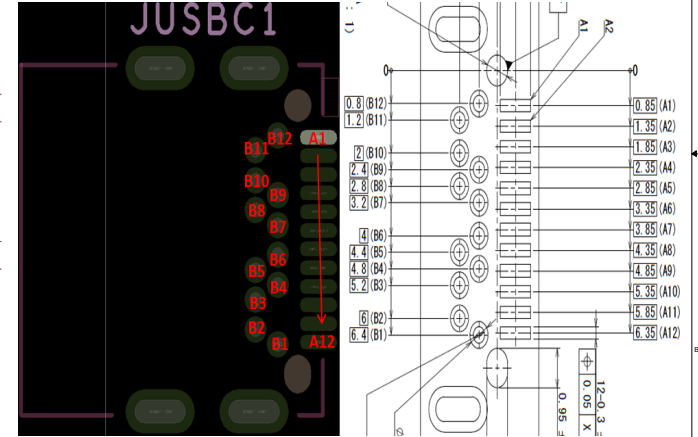
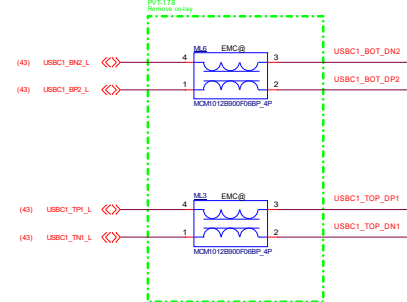
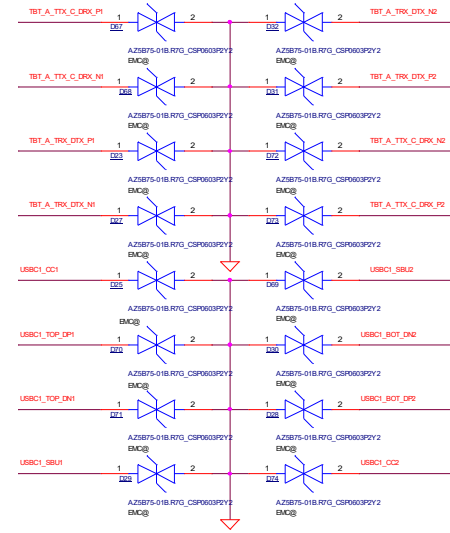
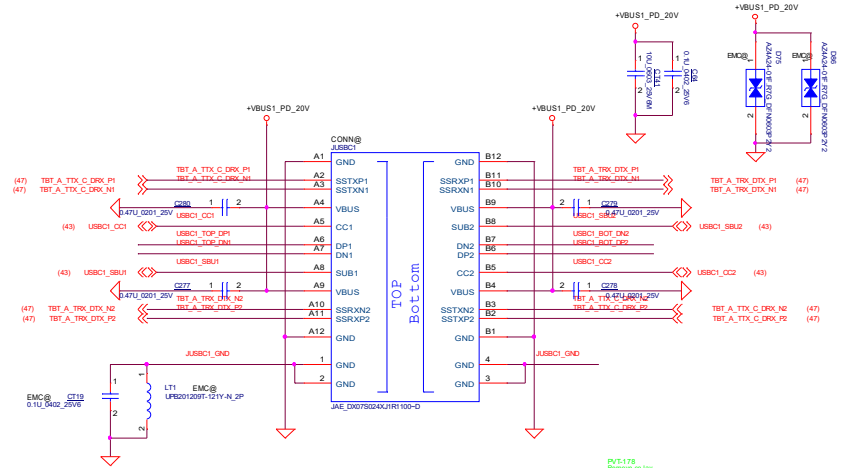


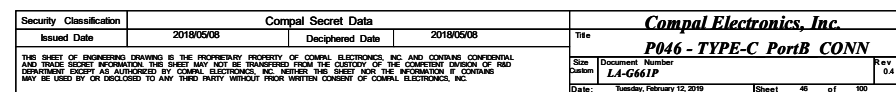
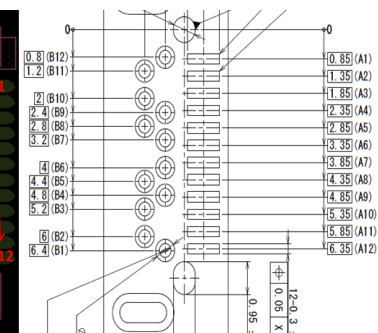
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20	3	DGND	23	4	MIC_select
19	5	DGND	24	6	MIC_3V3
18	7	MCLK	25	8	MIC_GND
17	9	DGND	26	10	MIC_CLK
16	11	DGND	27	12	MIC_DATA
15	13	DATA3_N	28	14	DGND
14	15	DATA3_P	29	16	DVDD
13	17	DGND	30	18	DGND
12	19	DATA1_N	31	20	AGND
11	21	DATA1_P	32	22	AVDD
10	23	DGND	33	24	DGND
9	25	CLK_N	34	26	SCL
8	27	CLK_P	35	28	SDA
7	29	DGND	36	30	DGND
6	31	DATA0_N	37	32	DOVDD
5	33	DATA0_P	38	34	PWDN
4	35	DGND	39	36	DGND
3	37	DATA2_N	40	38	VCM_VDD28
2	39	DATA2_P	41	40	VCM_GND
1	41	DGND	42	42	DGND
43	46	DGND	44	45	DGND
45	43	DGND	46	44	DGND

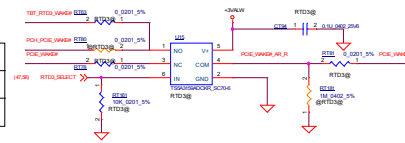
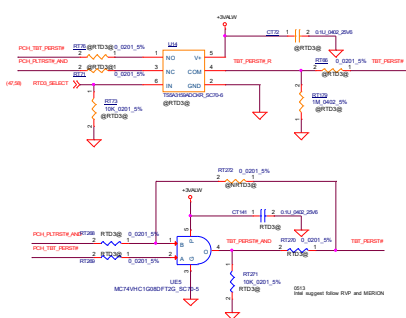
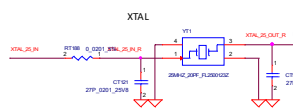
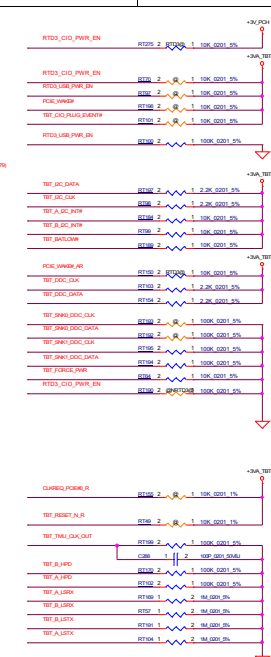
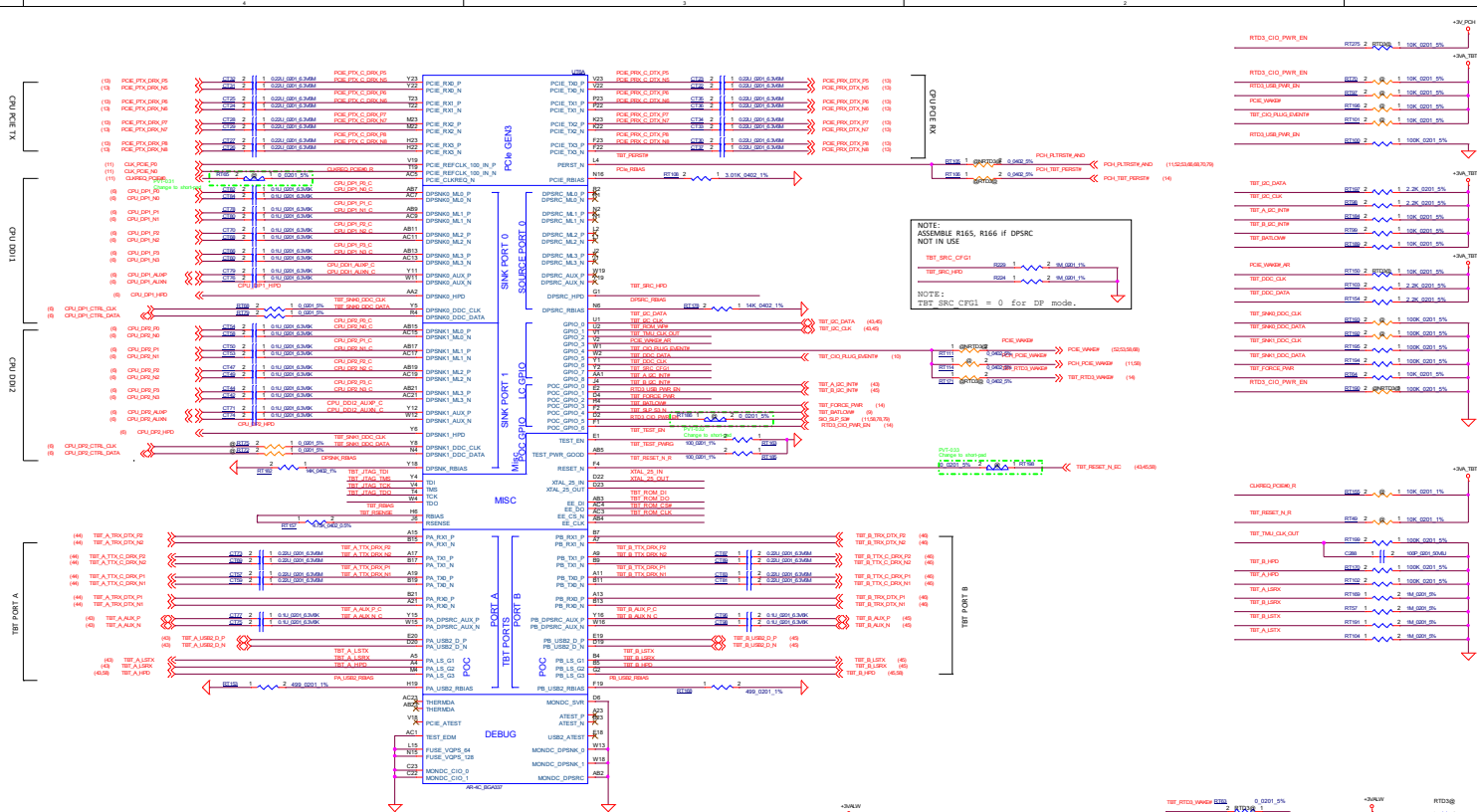
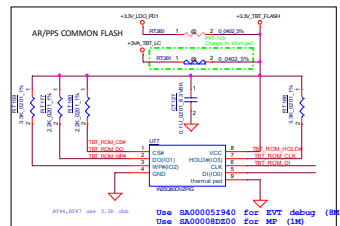
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				Size	Document Number LA-G661P
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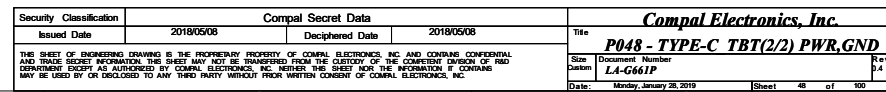


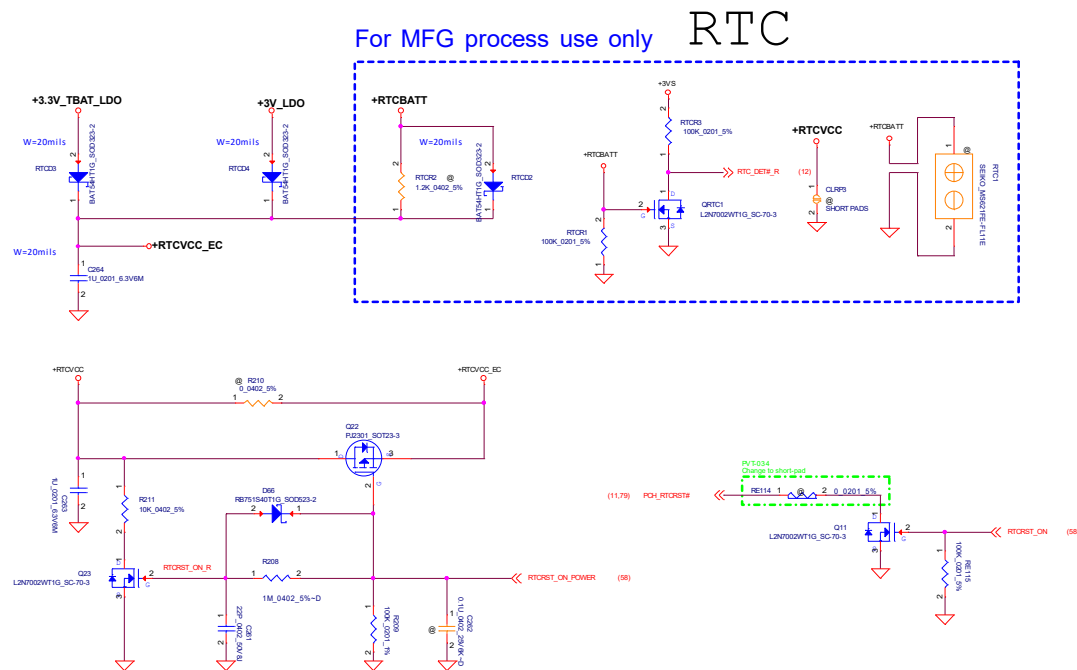
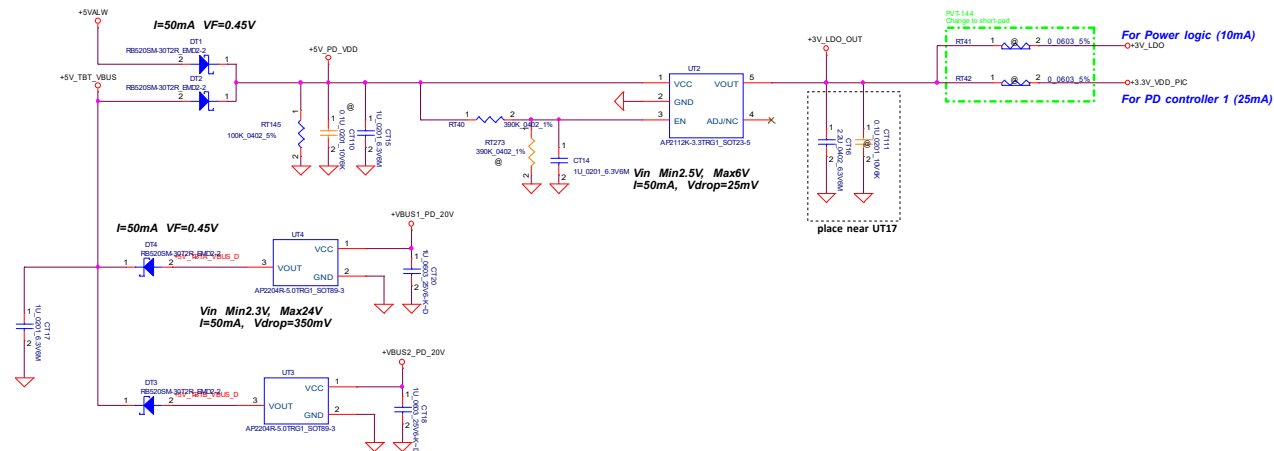




IN	NC	NO
L	COM	X
H	X	COM

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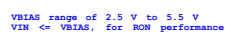
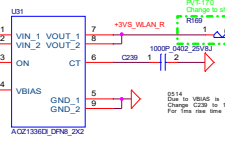
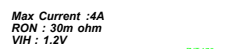
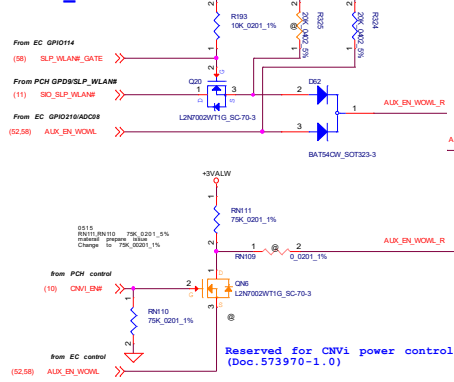
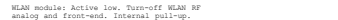
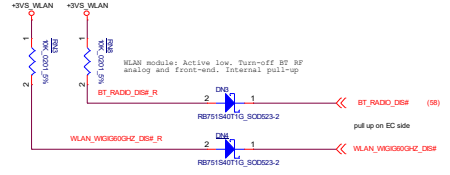
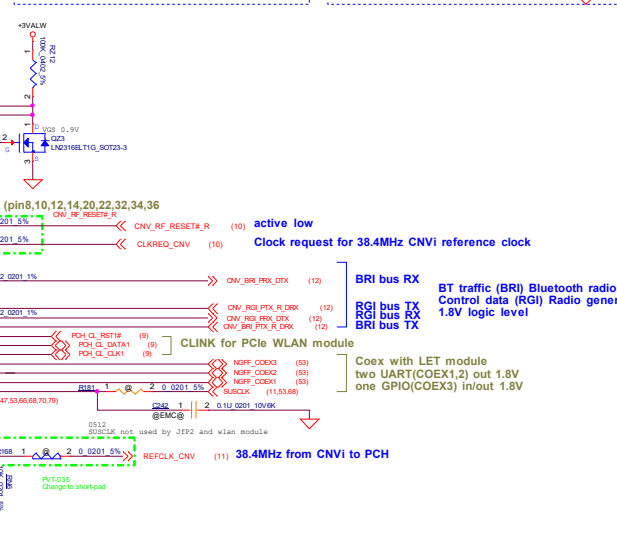
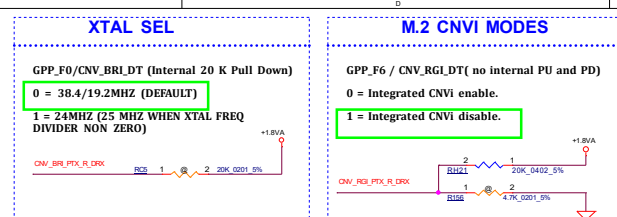
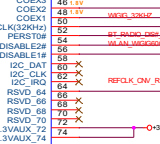
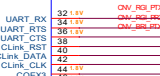
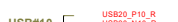
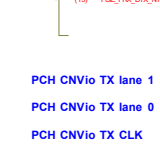
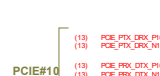
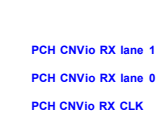
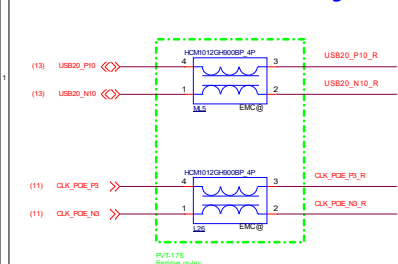


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				Size	Document Number	Rev
				LA-G661P		0.4
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		Document Number			0.4
Date:		Monday, January 28, 2019		Sheet	51 of 100

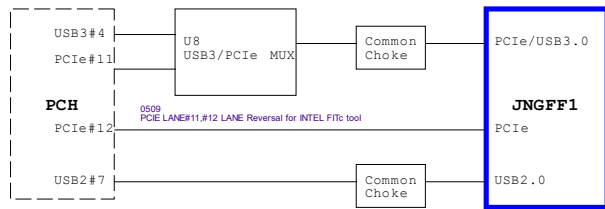
WLAN/BT/CNVi/PCIe
M.2 2230 Key-E



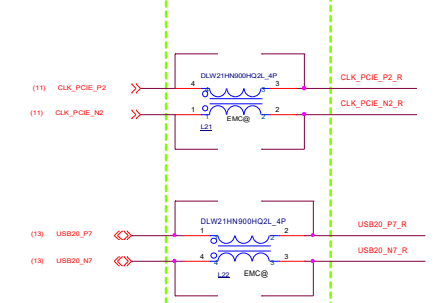
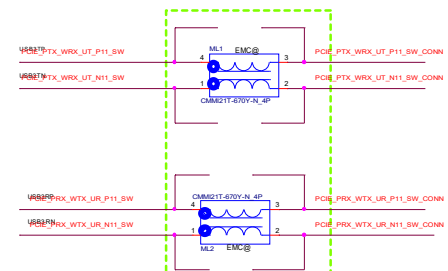
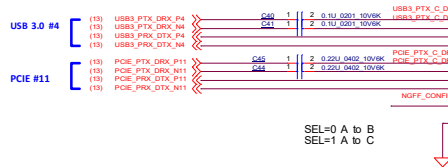
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Issued Date	20180508	Deciphered Date	20180508	P052 - WLAN/BT (w/ CNVI)		
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WWAN USB or 2nd SSD PCIe

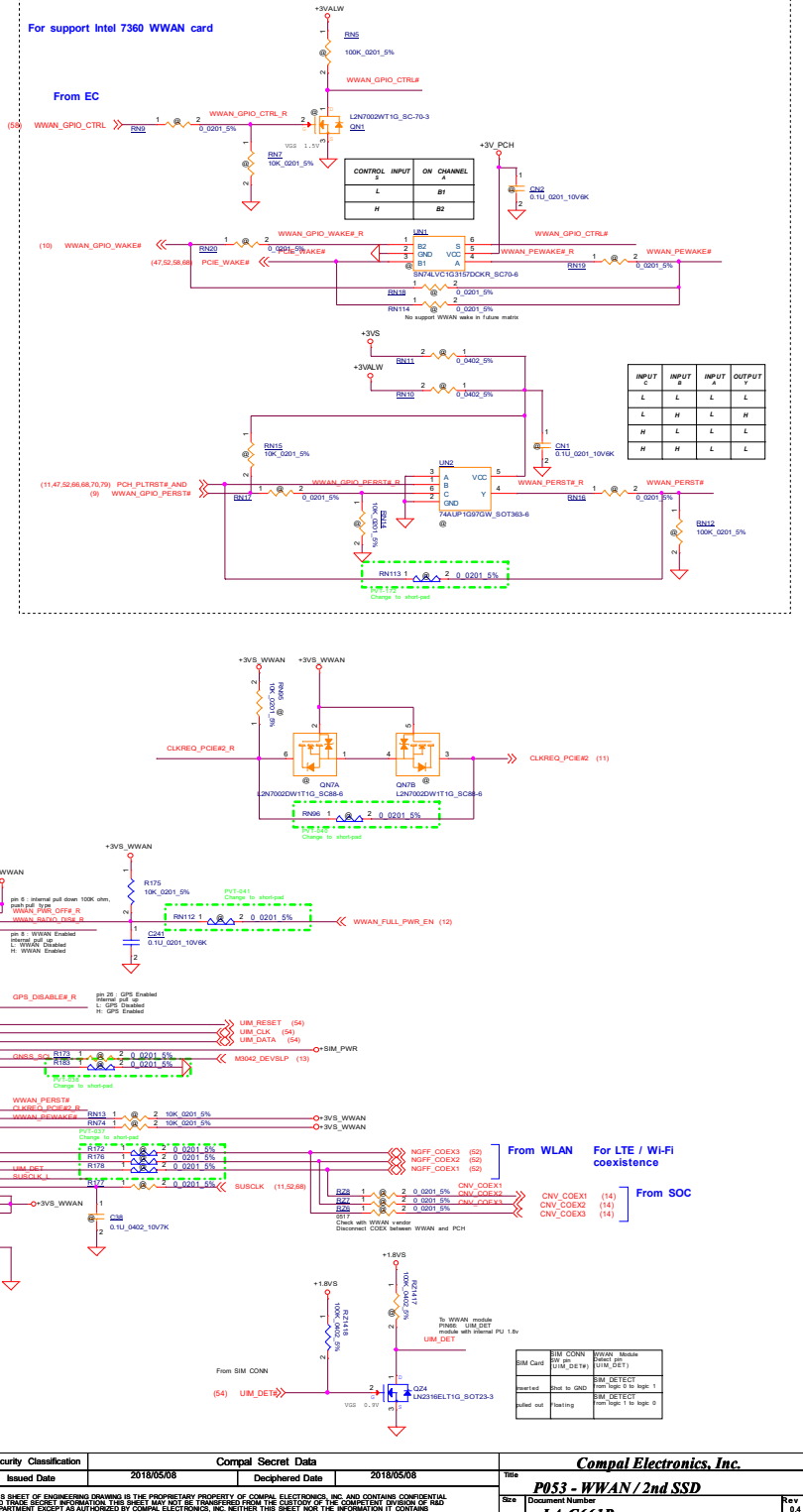
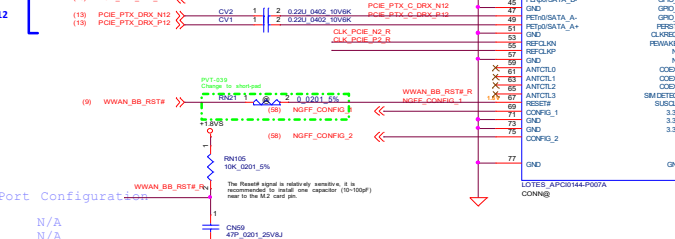
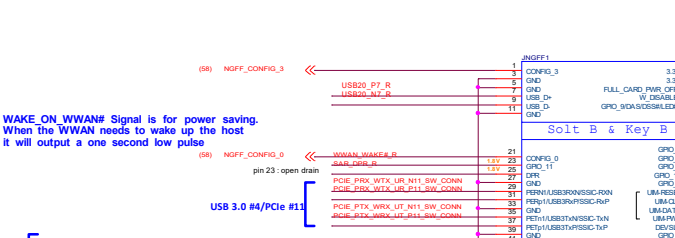
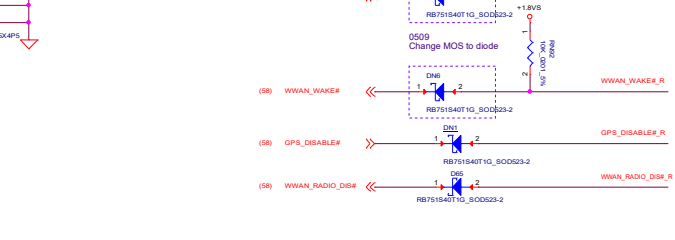
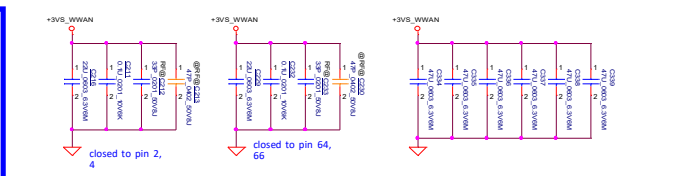
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


PCIe/USB 3.0 Mux

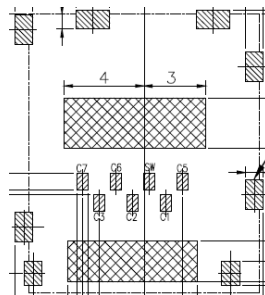
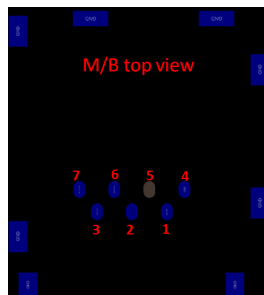


State#	CONFIG 0 (Pin 21)	CONFIG 1 (Pin 69)	CONFIG 2 (Pin 75)	CONFIG 3 (Pin 1)	Module Type	Port Configuration
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	HIGH	GND	GND	SSD - PCIe	N/A
2	GND	HIGH	GND	HIGH	WWAN - PCIe	1
3	GND	HIGH	HIGH	GND	WWAN - PCIe	0
4	GND	HIGH	GND	HIGH	WWAN - USB 3.0	0
5	GND	HIGH	GND	HIGH	WWAN - USB 3.0	1
6	GND	GND	HIGH	HIGH	WWAN - USB 3.0	2
7	GND	HIGH	HIGH	HIGH	WWAN - USB 3.0	3
8	HIGH	GND	GND	GND	WWAN - SSIC	0
9	HIGH	GND	GND	GND	WWAN - SSIC	2
10	HIGH	HIGH	HIGH	GND	WWAN - SSIC	3
11	HIGH	GND	GND	HIGH	WWAN - PCIe	2
12	HIGH	GND	GND	HIGH	WWAN - PCIe	3
13	HIGH	HIGH	GND	HIGH	DDP/HCA - PCIe	N/A
14	HIGH	GND	HIGH	HIGH	DDP/HCA - PCIe	N/A
15	HIGH	HIGH	HIGH	HIGH	No Module	N/A



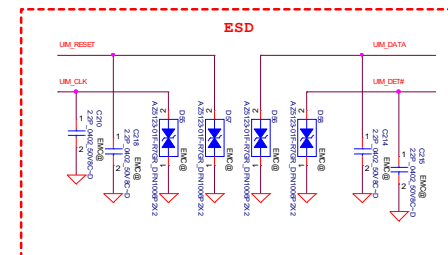
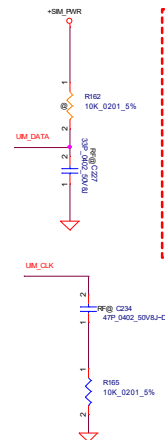
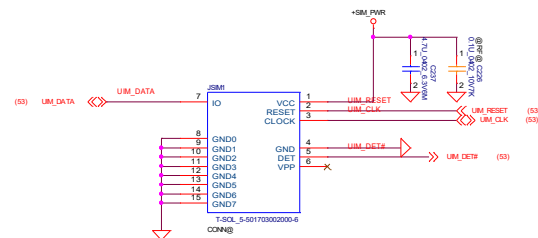
COMPOSITION OF DETECTION	
CARD DETECT(SW)	
C5  SW	
CARD DETECTION/SWITCH	
CARD INSTALLATION:ON	
NON CARD:OFF	

NANO SIM normal Open CONN.
 No Card: SW floating
 Card install: SW shot to GND(C5)



SIM Card Pin Assignments

NANO	SIM	CARD
C1		Vcc
C2		RST
C3		CLK
C5		GND
SW		CD/SW
C6		Vpp
C7		DATA

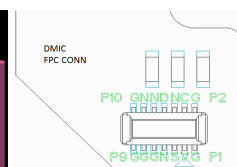
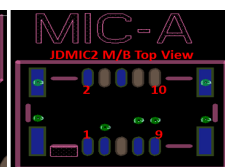
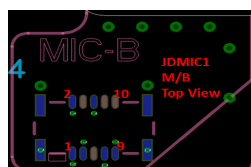
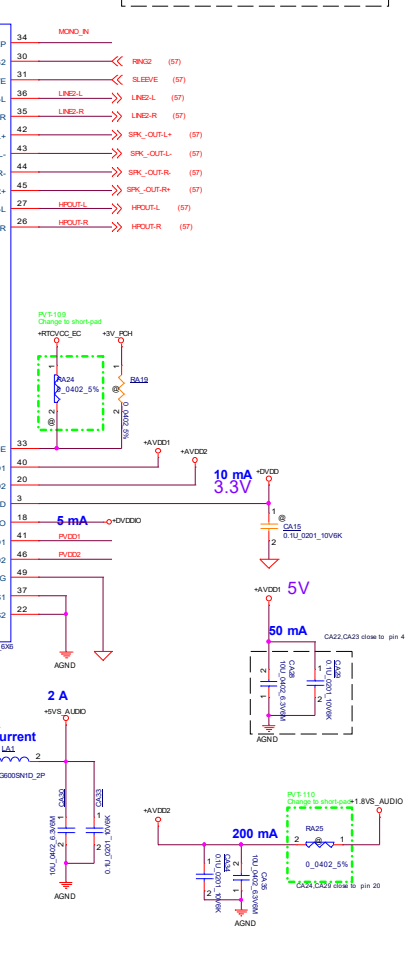
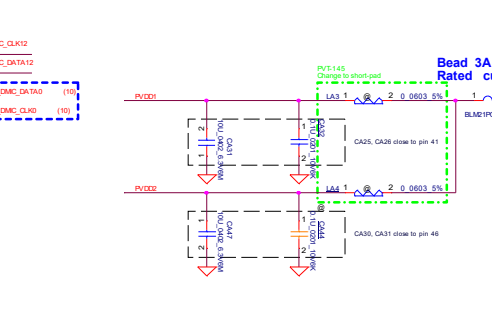
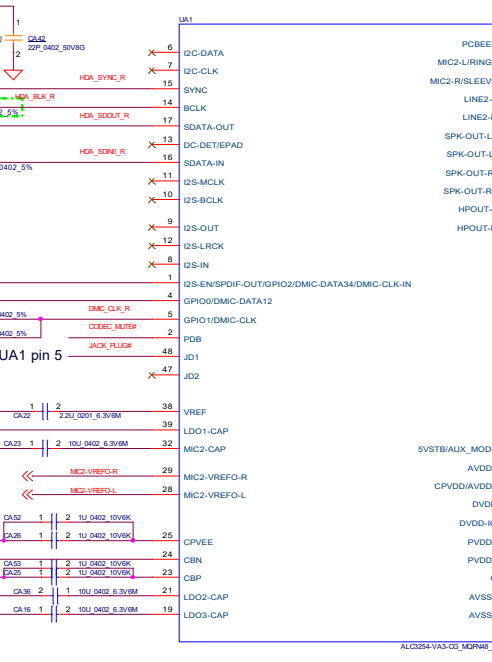
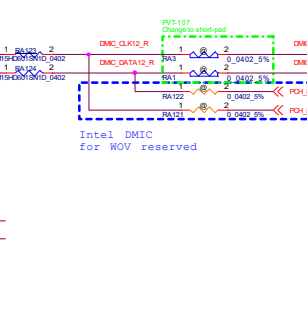
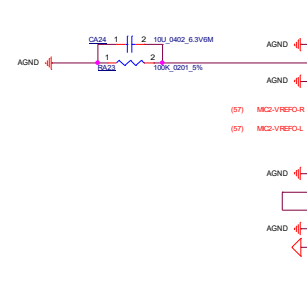
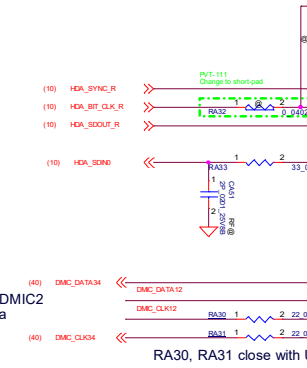
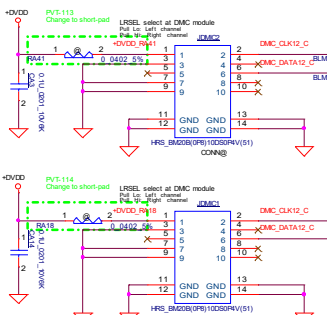
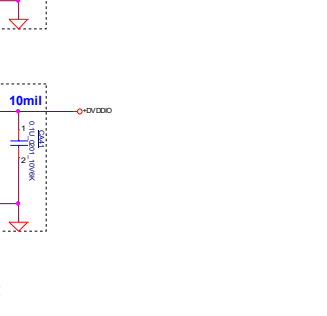
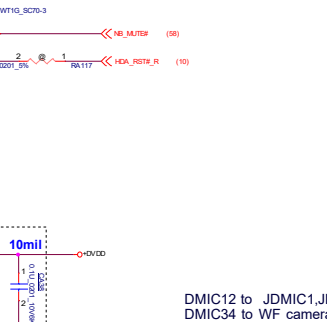
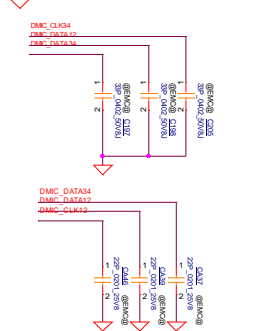
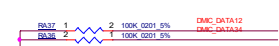
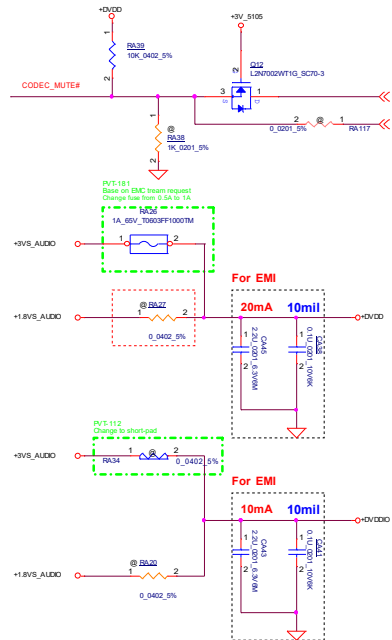
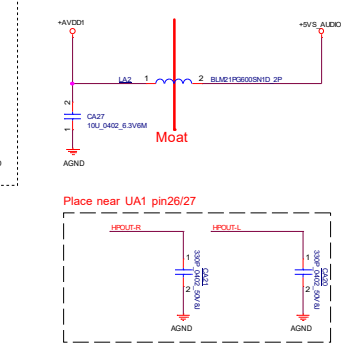


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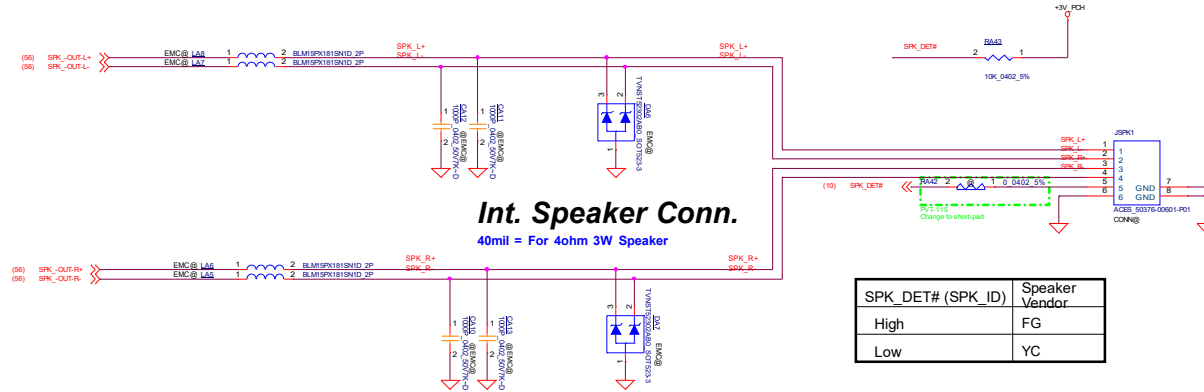
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				Size	Document Number	Rev
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Date	Version		2019	Sheet	56 of 100

Int. Speaker Conn.

40mil = For 4ohm 3W Speaker

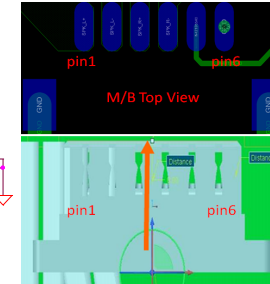


FG

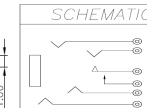
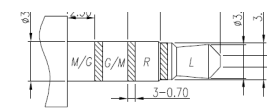
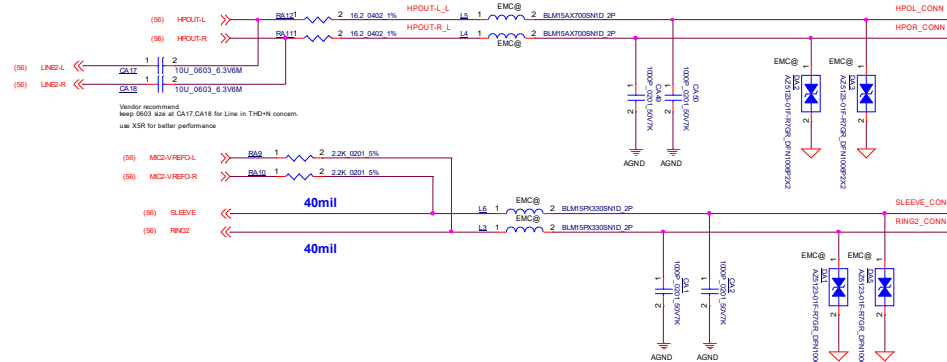
Conn Pin	Net name	Cable color
Pin 6	N/A	N/A
Pin 5	N/A	N/A
Pin 4	SPK R-	Black
Pin 3	SPK R+	Red
Pin 2	SPK L-	Blue
Pin 1	SPK L+	White

YC

Conn Pin	Net name	Cable color
Pin 6	Loop with 5	Green
Pin 5	Loop with 6	Green
Pin 4	SPK R-	Black
Pin 3	SPK R+	Red
Pin 2	SPK L-	Blue
Pin 1	SPK L+	White

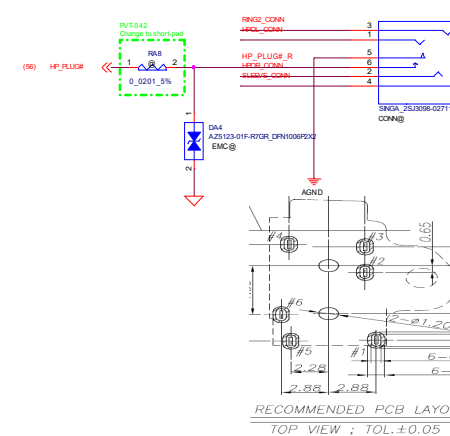


Universal Audio Jack

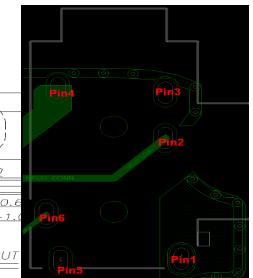


Singapore Enterprise Co., Ltd.	
信晉企業股份有限公司	
TITLE	#3.50 AUDIO JACK
OWN	Qing PARE NO.2S3098-027111F
CHKD	Brace SCALE 4:1 UNIT: mm
APVD	Loop SIZE: A3 SHEET: 1 OF 1 REV: 4
CUSTOMER COPY	

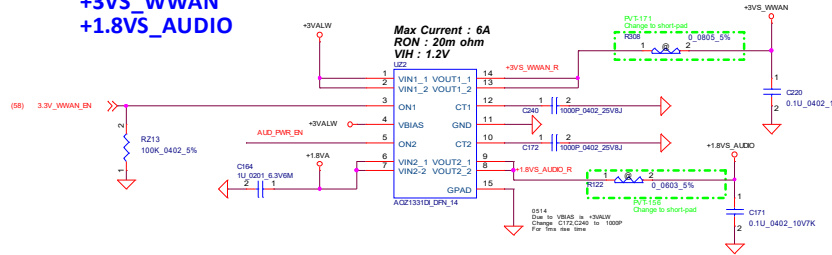
Universal Audio Jack CONN



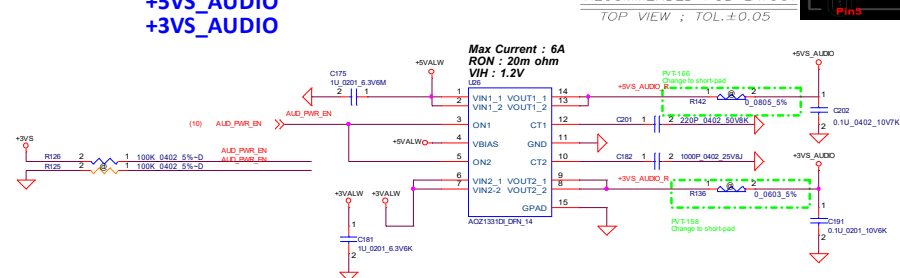
Audio Signal	Audio Conn	Pin
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HPOL_CONN	#1 LR	
HPOR_CONN	#2 RL	
SLEEVE_CONN	#4 MG	
HP_PLUG#_R	#5	
AGND	#5	



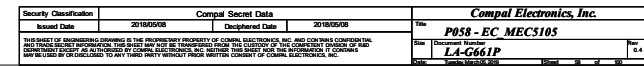
+3VS_WWAN
+1.8VS_AUDIO



+5VS_AUDIO
+3VS_AUDIO

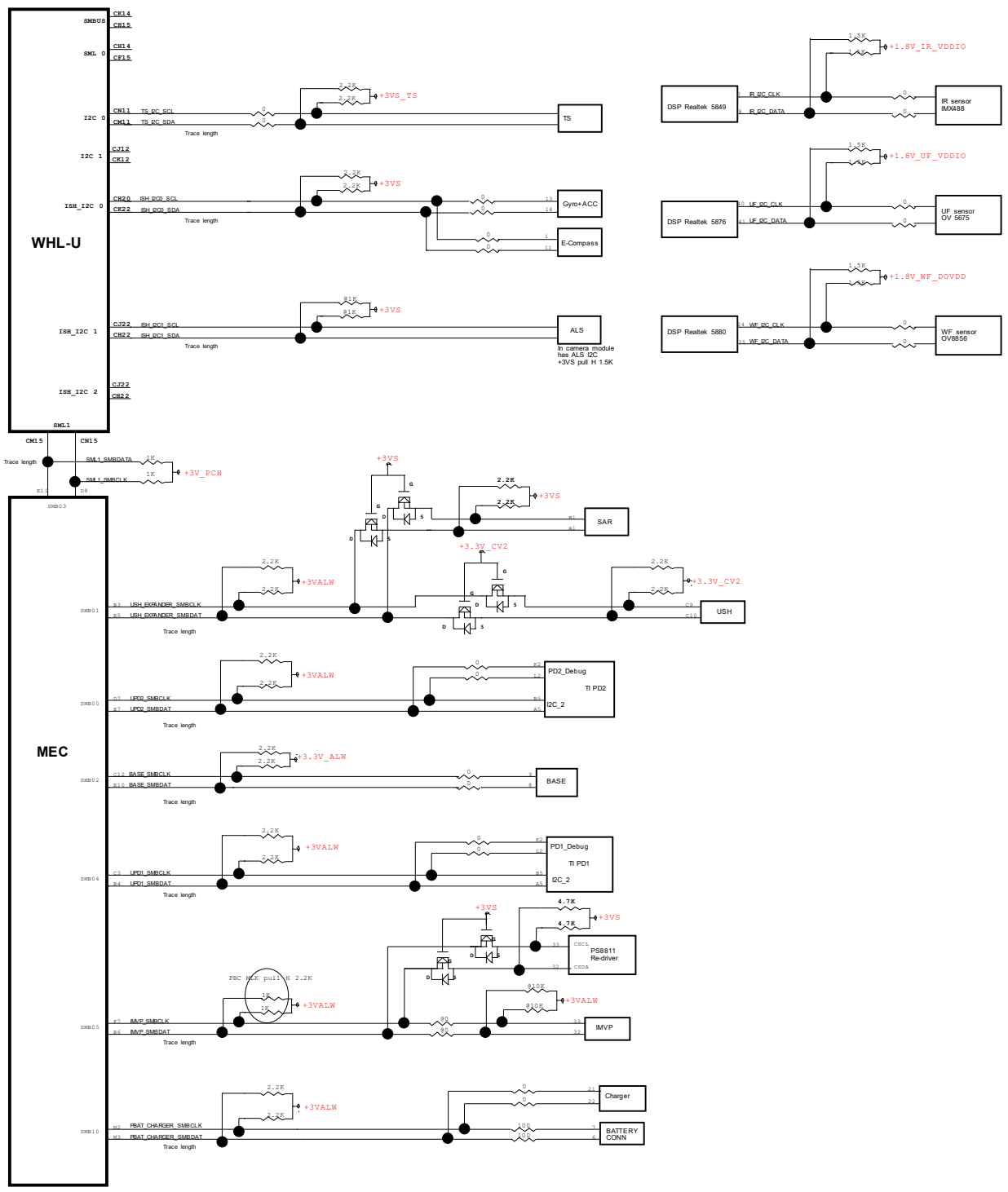


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Date: Monday, January 28, 2019		Sheet 50 of 100																											
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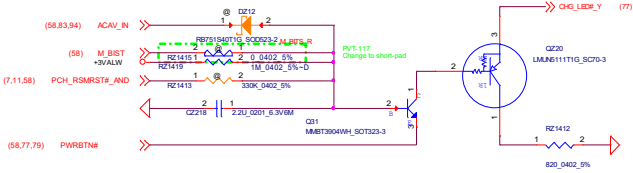
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Date: Monday, January 28, 2019				Sheet 60 of 100																									
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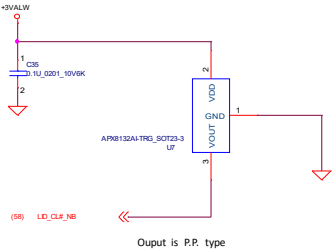
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				Date:	Monday, January 28, 2019	Sheet 62 of 100

M-BITS



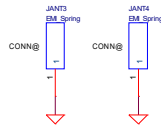
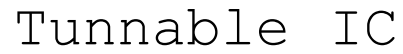
Hall sensor



Magnetic field enters the Hall sensor, output turns on (output is high)
Magnetic field release point, output turns off (output is high)

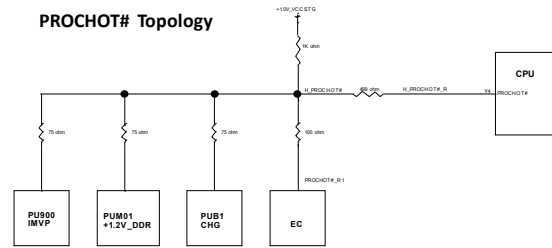
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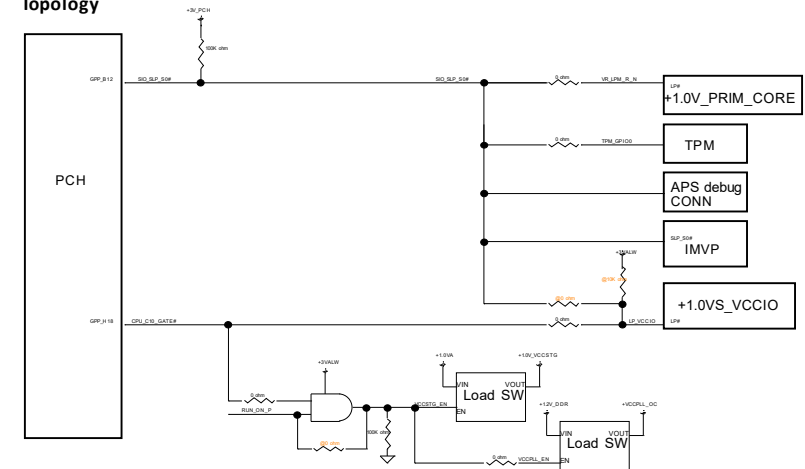


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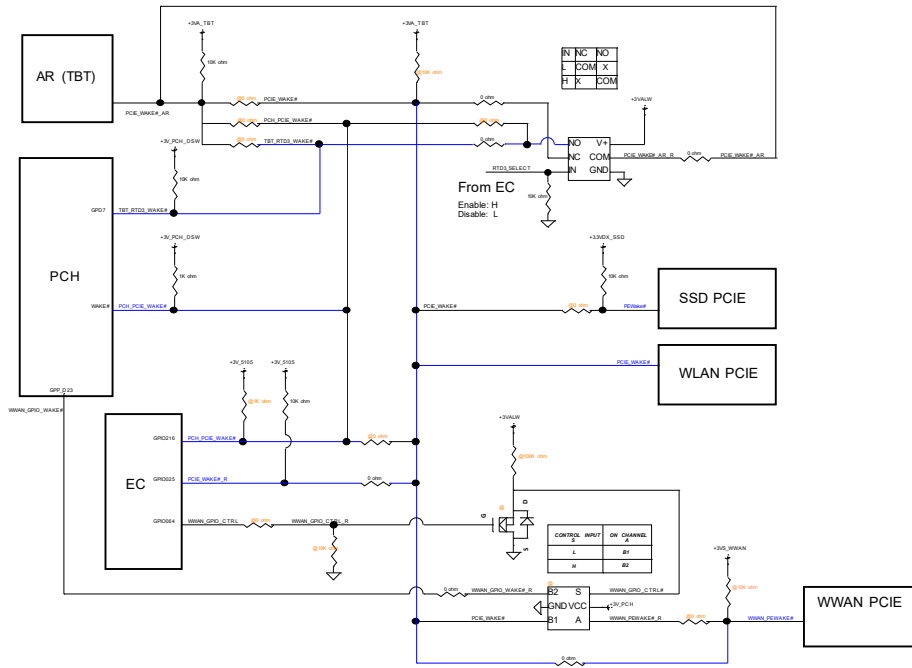
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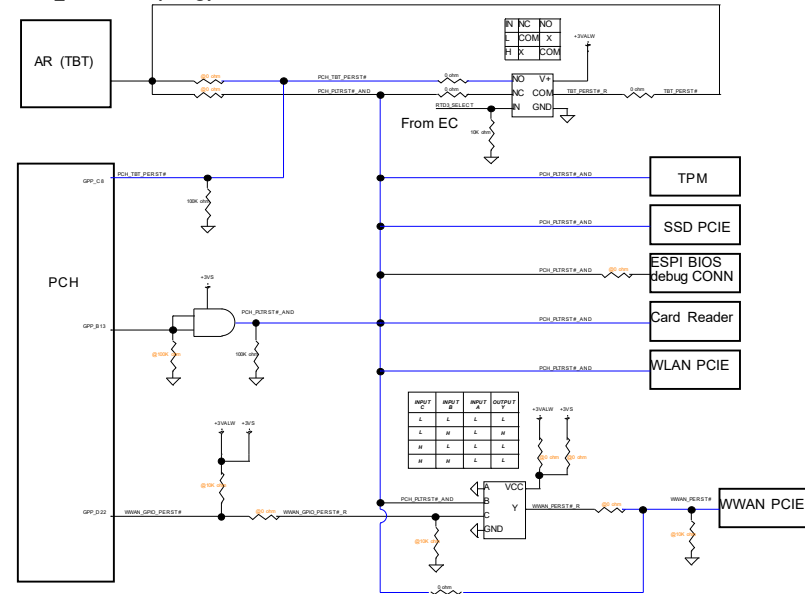
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PCH_PCIE_WAKE# Topology



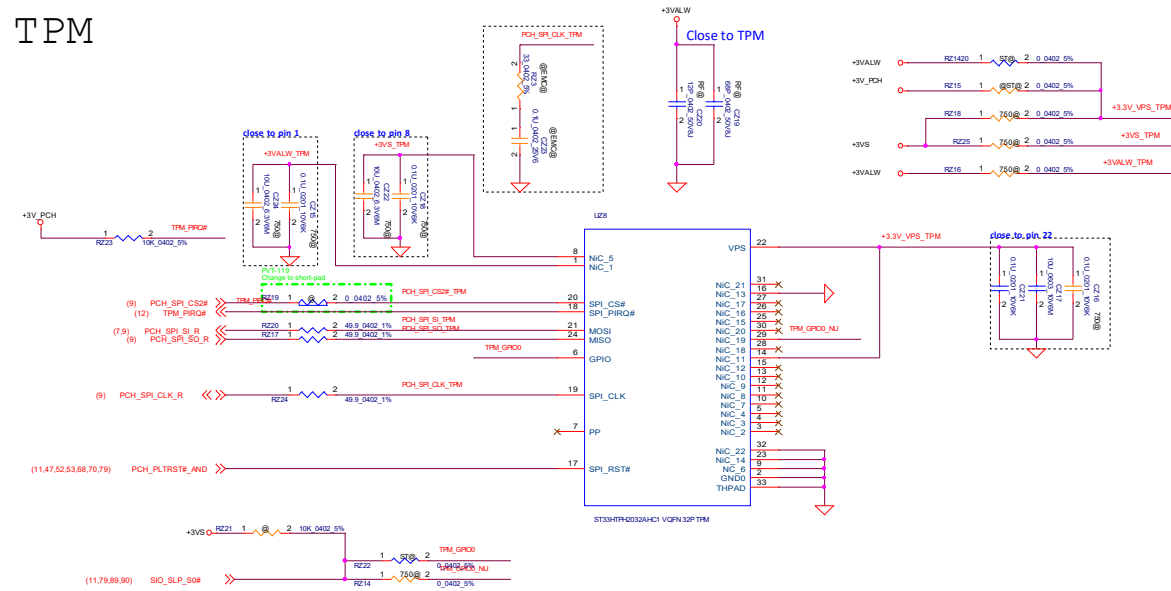
PCH_PLTRST# Topology



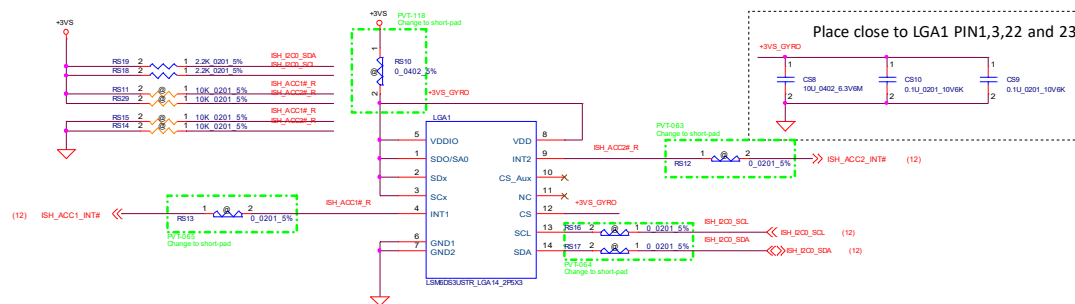
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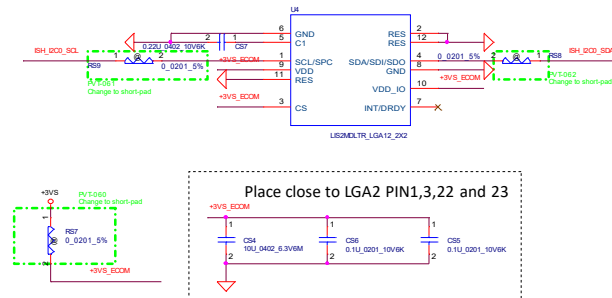
TPM



3D accelerometer and 3D gyroscope

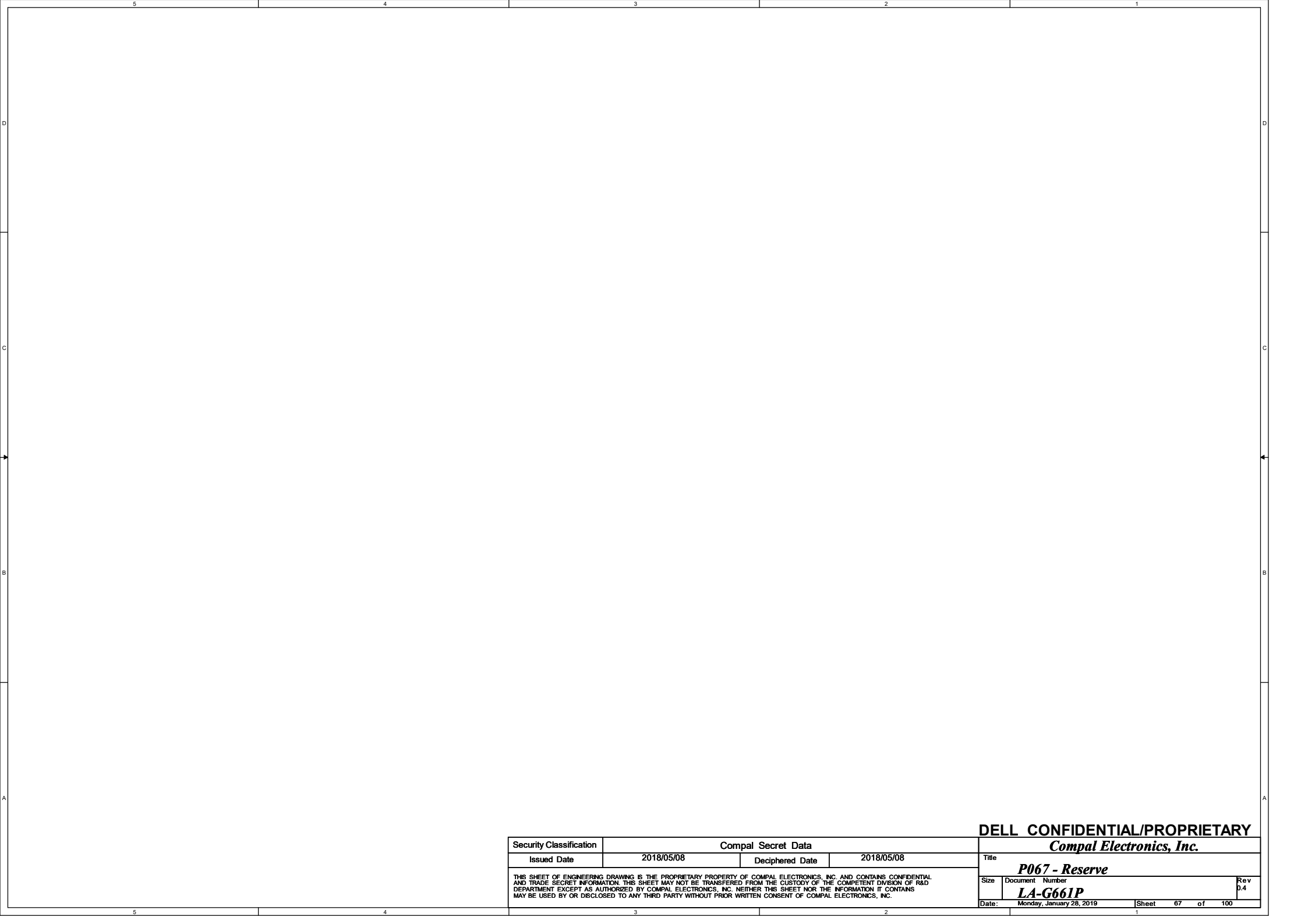


E-Compass

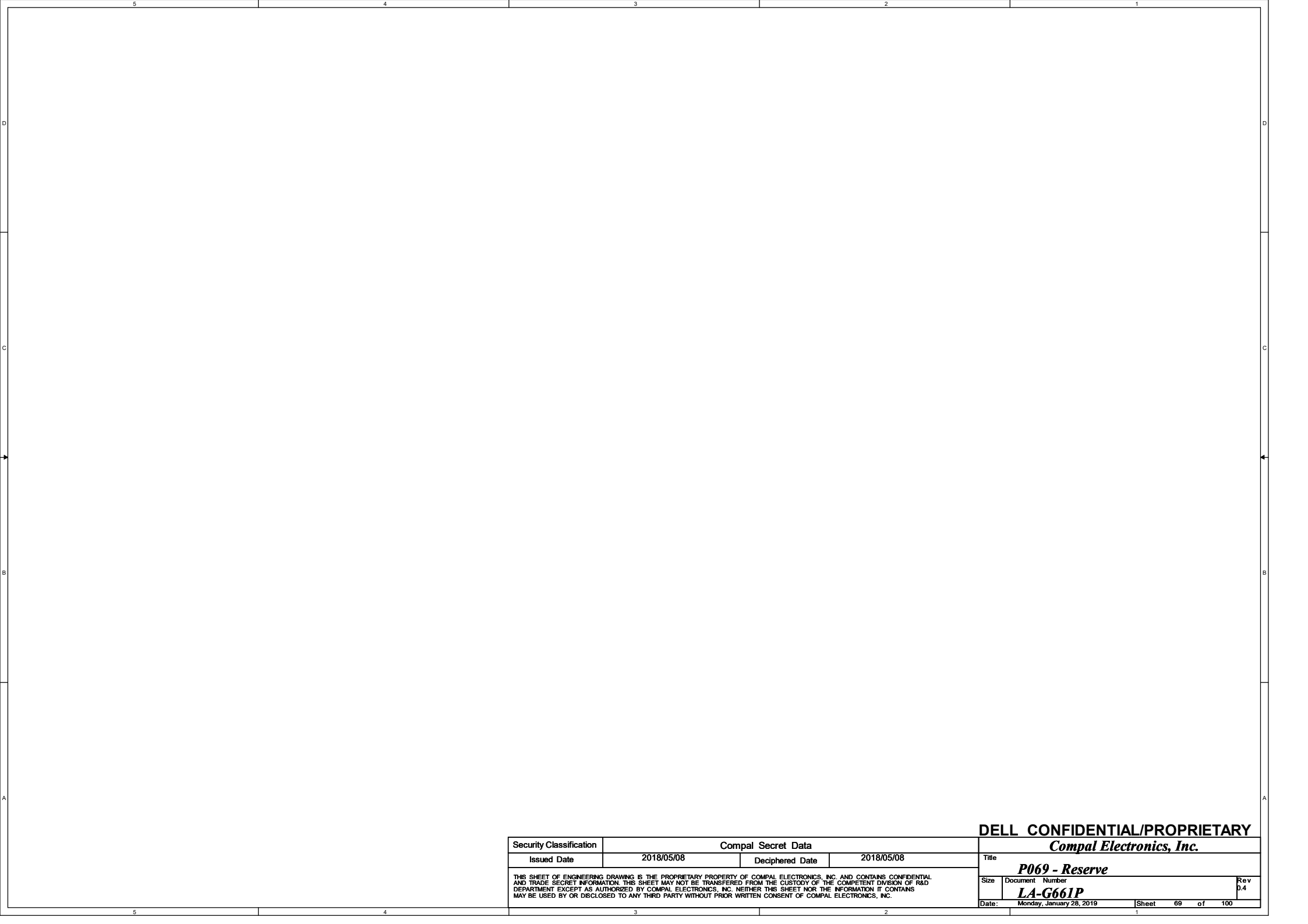


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		LA-G661P			0.4
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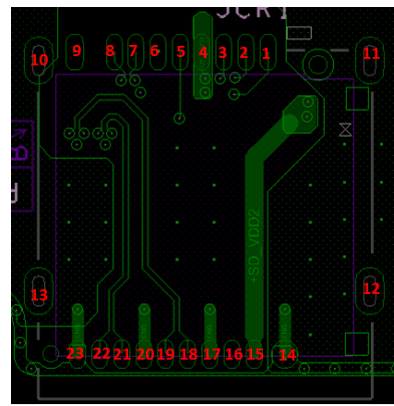
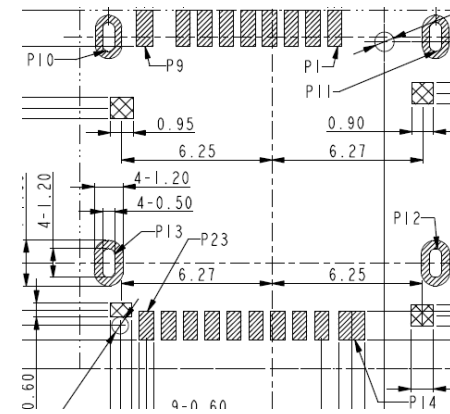
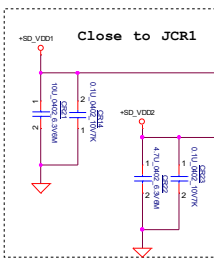
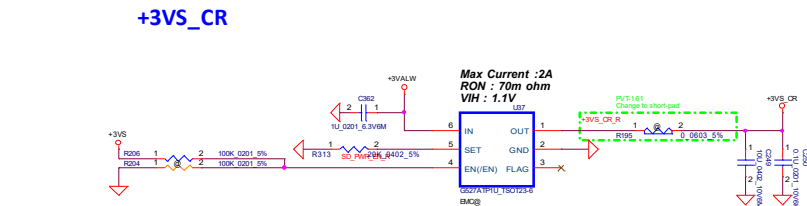
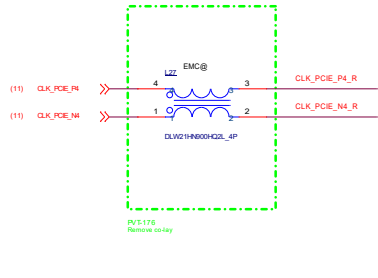
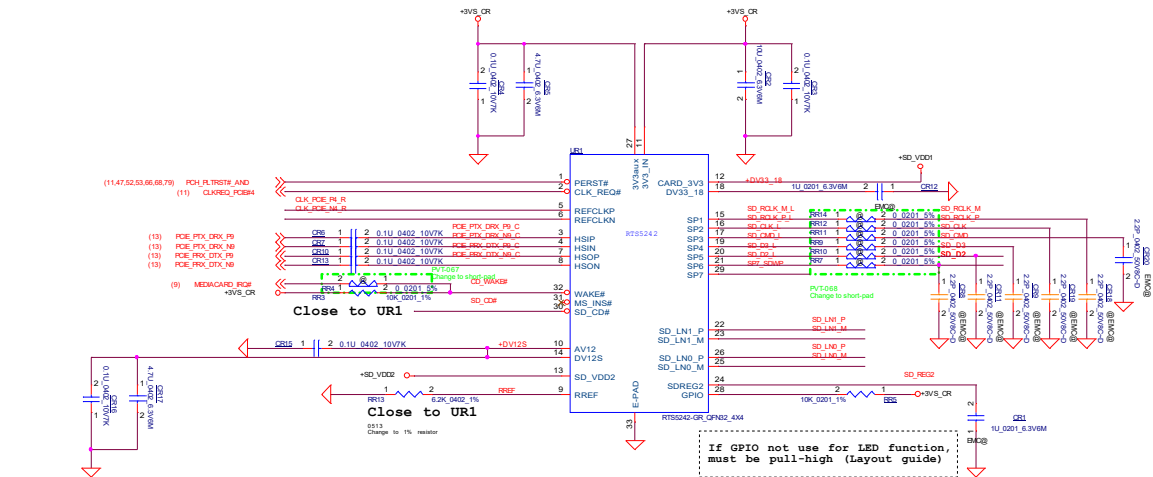


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D				D
C				C
B				B
A				A

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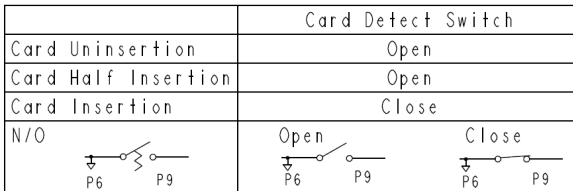
Card Reader

- 1)Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
- 2)Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
 - Bulk capacitor for Card 3V3 place closed to flash card socket.
 - Bulk capacitor for 3V3 IM / 3V3aux / DV12S place closed to RTS5242 chip.
- 3)Keep damping resistor (ex. for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
- 4)Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.



Pin No.	Pin Assignment
P1	MICRO SD DAT2
P2	MICRO SD CD/DAT3
P3	MICRO SD CMD
P4	MICRO SD VDD1
P5	MICRO SD CLK
P6	MICRO SD VSS
P7	MICRO SD DAT0/RCLK+
P8	MICRO SD DAT1/RCLK-
P9	MICRO SD CD
P10	GND
P11	GND
P12	GND
P13	GND
P14	GND
P15	MICRO SD VDD2
P16	MICRO SD SWIO
P17	MICRO SD VSS
P18	MICRO SD DO+
P19	MICRO SD DO-
P20	MICRO SD VSS
P21	MICRO SD D1-
P22	MICRO SD D1+
P23	MICRO SD VSS

Opening/Close of Switch



TaiSol Electronics Co., Ltd.

MODEL: UNPC-TO-50

PART NAME: MICRO SD4.0 FOR S/D PUSH TOP MOUNT TYPE

PART NO.: 158-1090902601

TOL.: PLCP PLORWGL

MATERIAL: SEE NOTES

FINISH: SEE NOTES

DATE: 2018.06.20

DATE: 2018.06.20

DATE: 2018.06.20

APPROVED: JACKY

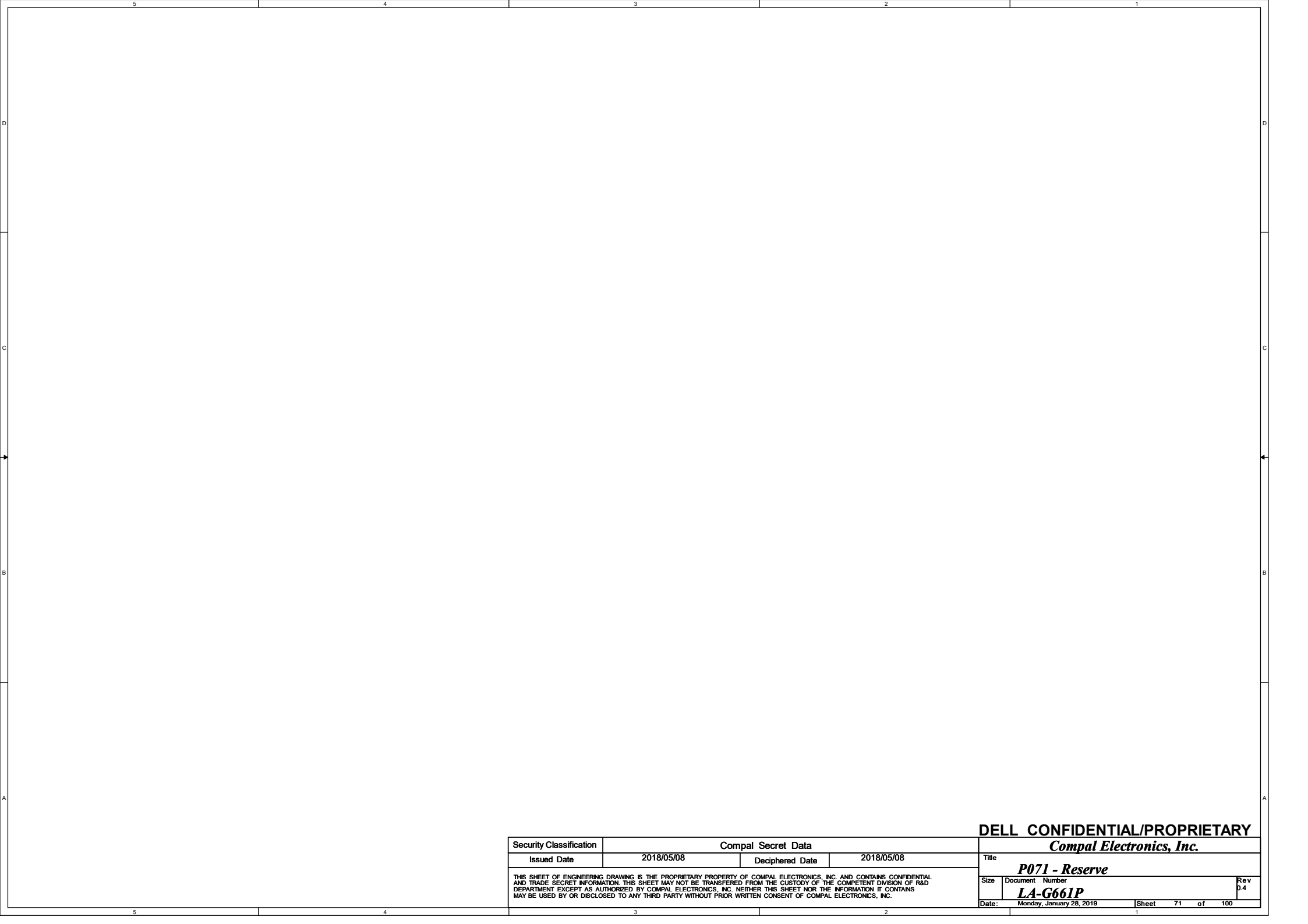
CHECKED: SUNNY

DRAWN: NICK

REV: 01

REV: 01

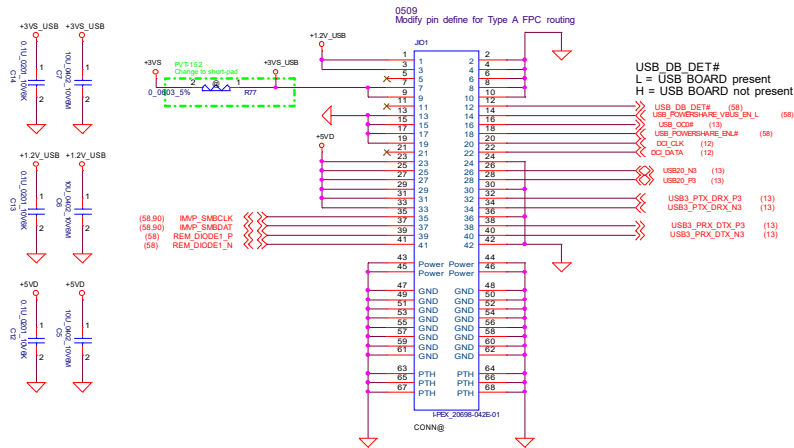
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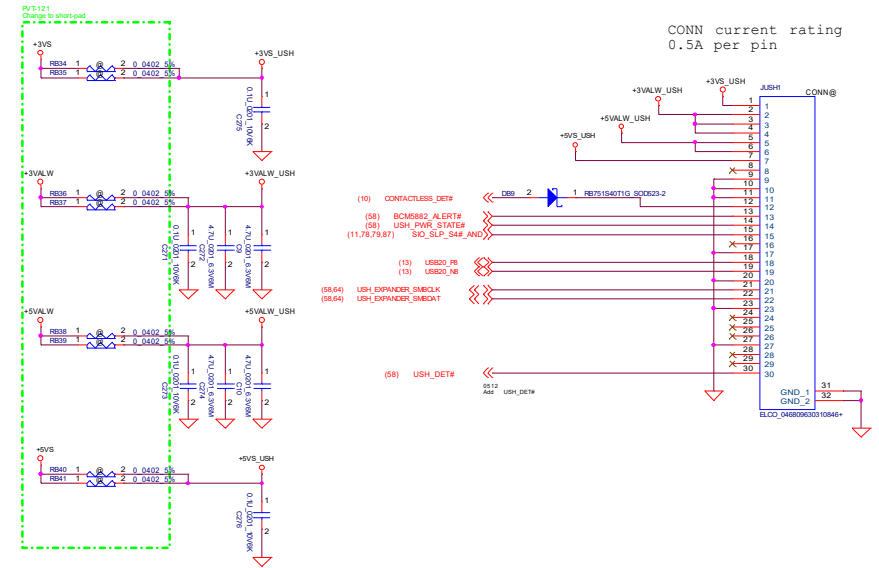
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				Size	Document Number	Rev
				LA-G661P		
				Date:	Monday, January 28, 2019	Sheet 71 of 100

5	4	3	2	1																														
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Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY																														
Issued Date		2018/05/08	Deciphered Date	2018/05/08	Title																													
					P072 - Reserve																													
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		Date: Monday, January 28, 2019			Sheet 72 of 100																													
5	4	3	2	1																														

USB Board CONN



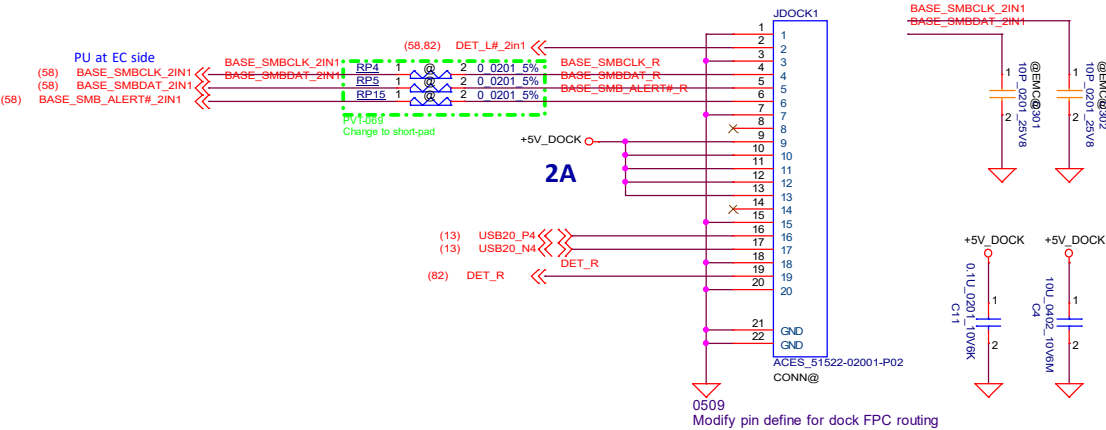
USH CONN.



DELL CONFIDENTIAL/PROPRIETARY

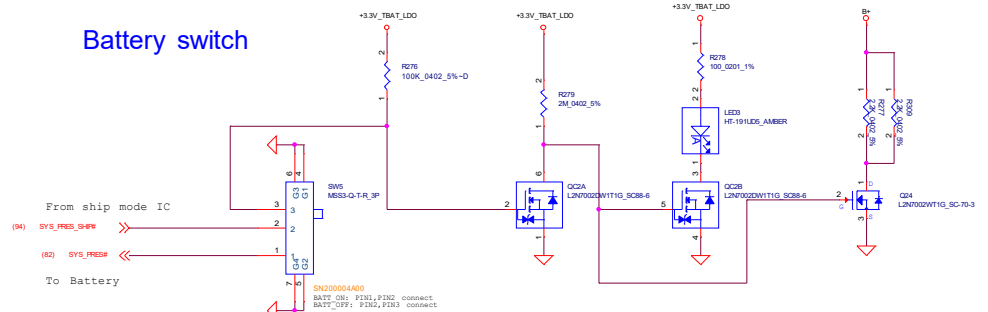
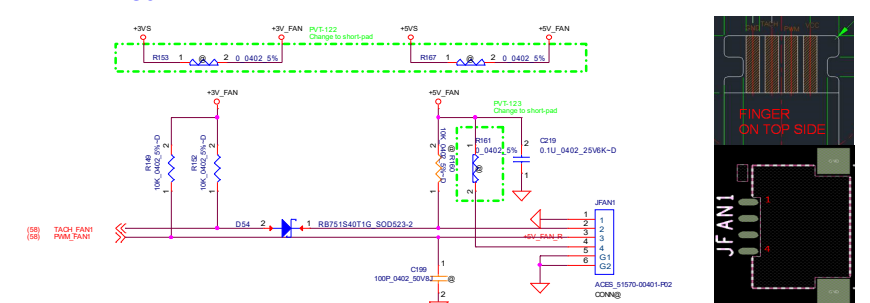
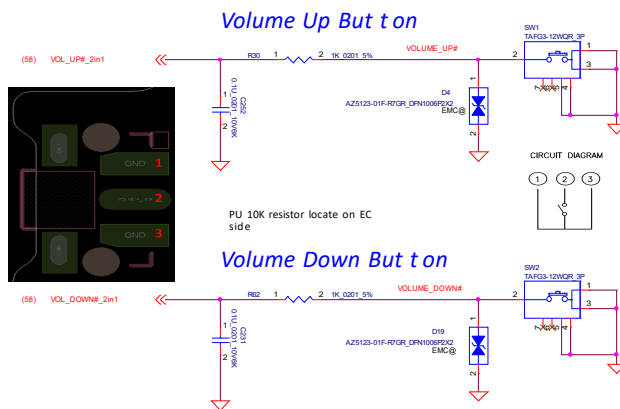
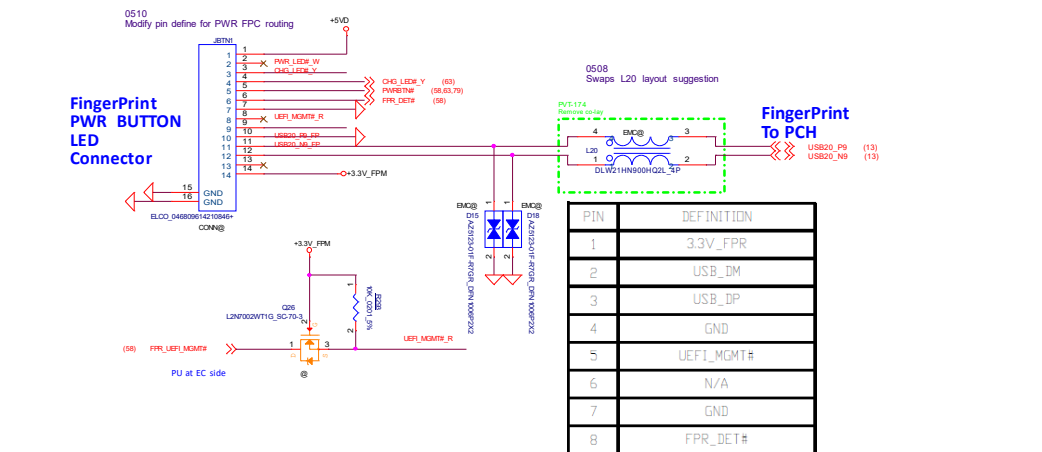
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Date: Thursday, January 31, 2019		Sheet		73 of 100	

Docking CONN



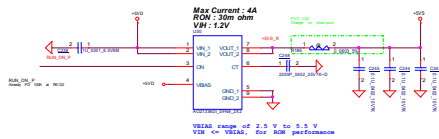
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Size		Document Number			Rev
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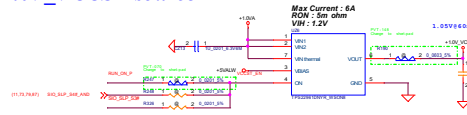


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Drawing Number LA-G661P				Date: Sunday, February 12, 2018	
				Sheet 77 of 100	

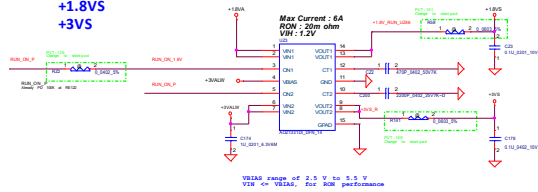
+5VS



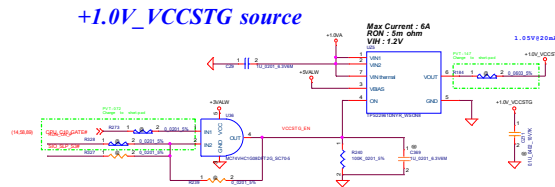
+1.0V_VCCST source



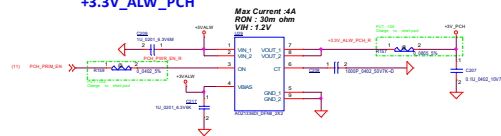
+1.8VS
+3VS



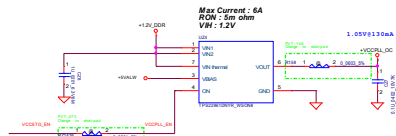
+1.0V_VCCSTG source



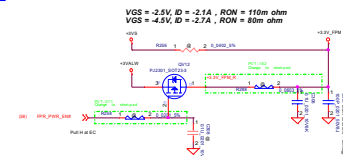
DSx
+3.3V_ALW_PCH



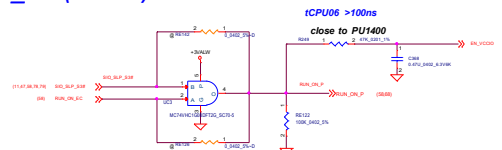
+VCCPLL_OC source (1.2V)



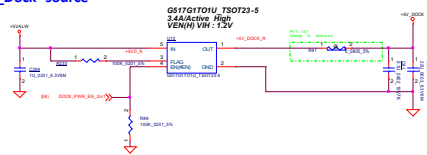
+3.3V_FPM



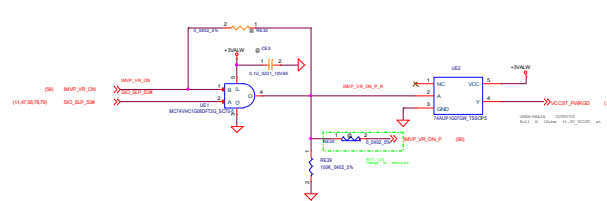
RUN_ON(VS EN)



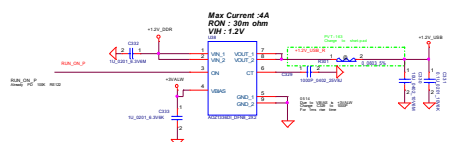
+5V_Dock source



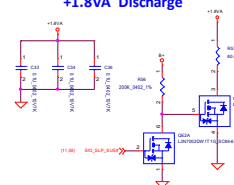
IMVP_VR_ON&VCCST_PWRGD



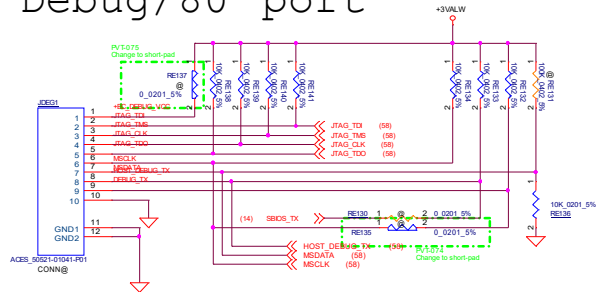
(+1.2V_USB) For Type A redriver



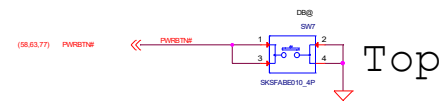
+1.8VA Discharge



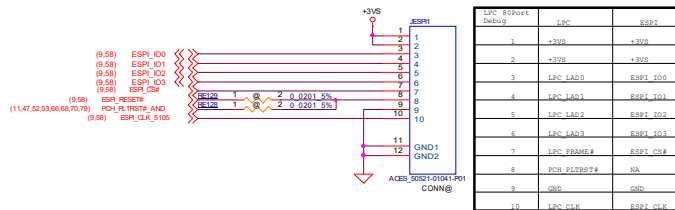
EC UART
Debug/80 port



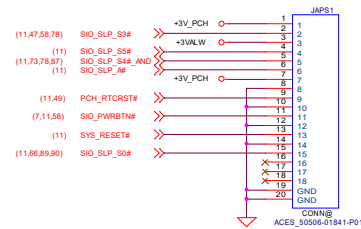
Test Power Button



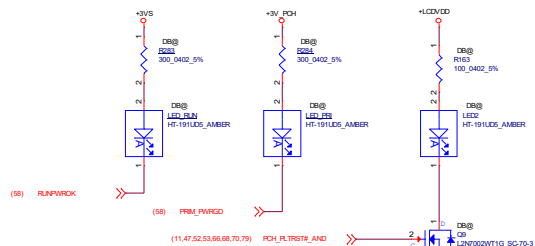
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ESPI
BIOS  debug
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APS CONN

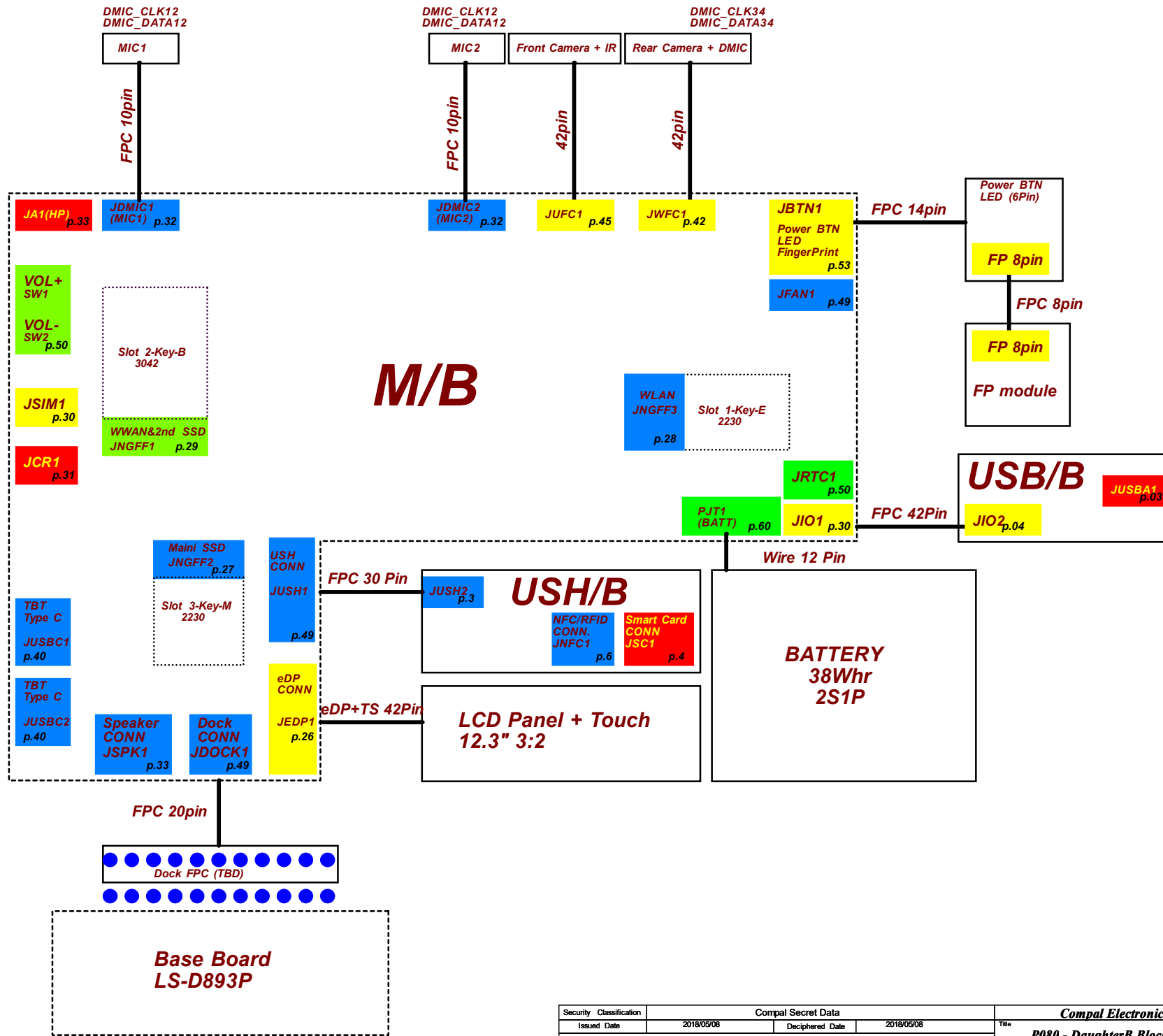


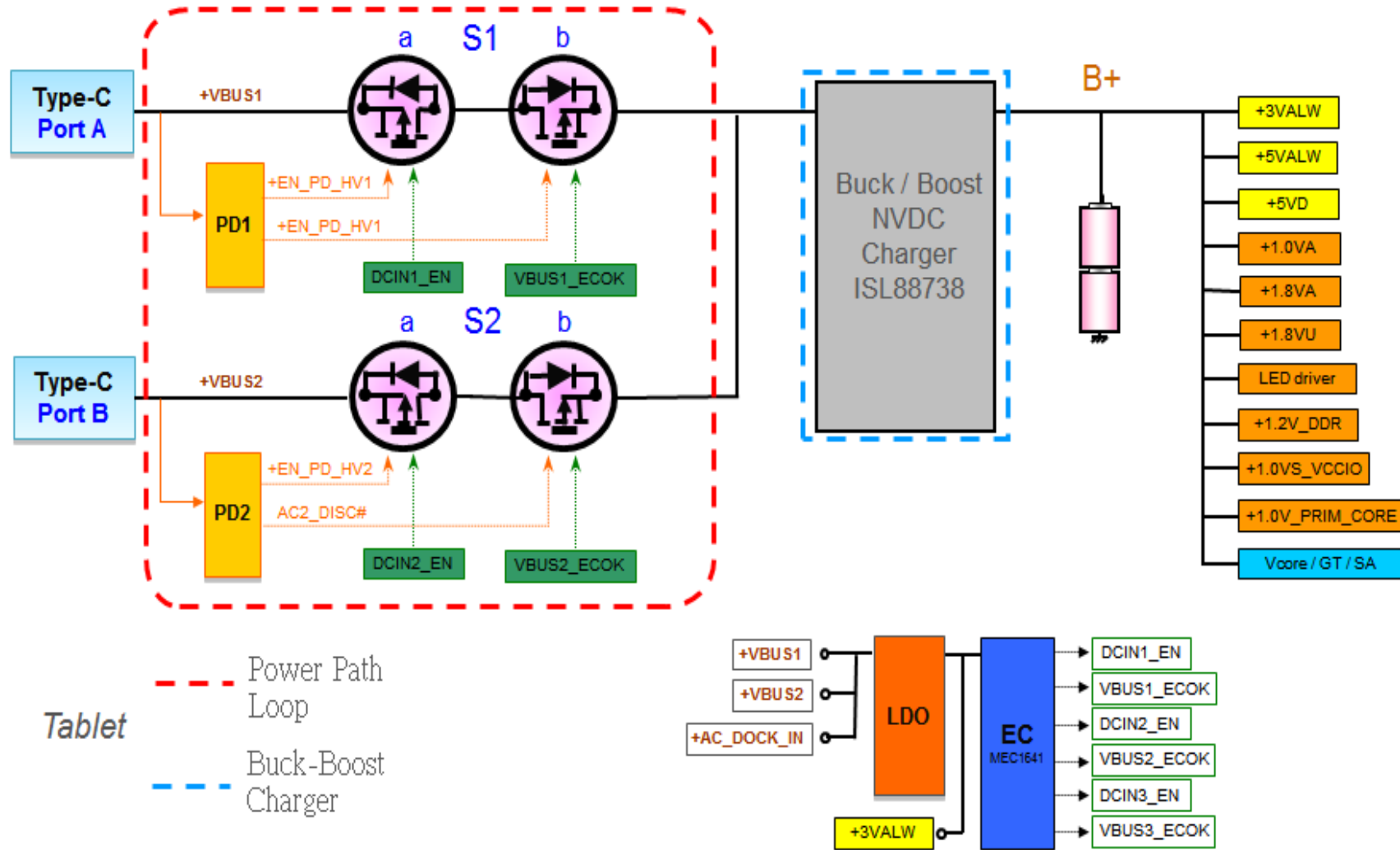
DEBUG LED



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				Date: Monday, January 28, 2019 Sheet 79 of 100	0.4

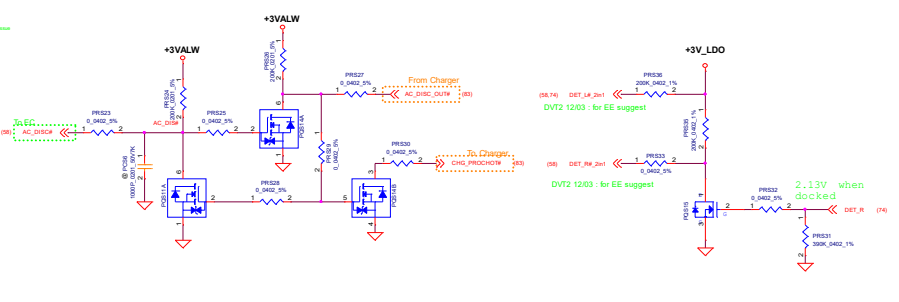
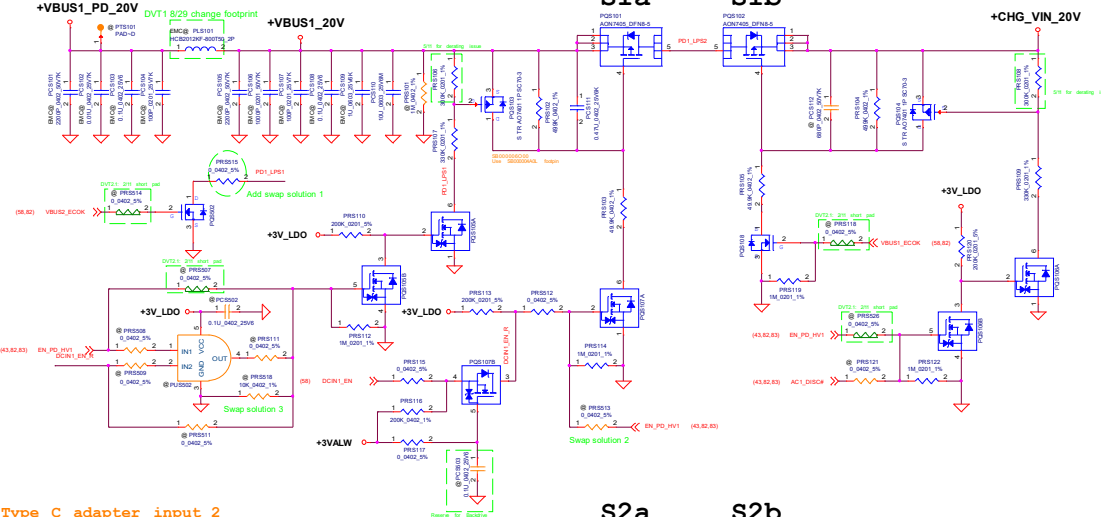
- New Tooling in DVT
- New applying
- Leverage others project
- Leverage PBC MLK



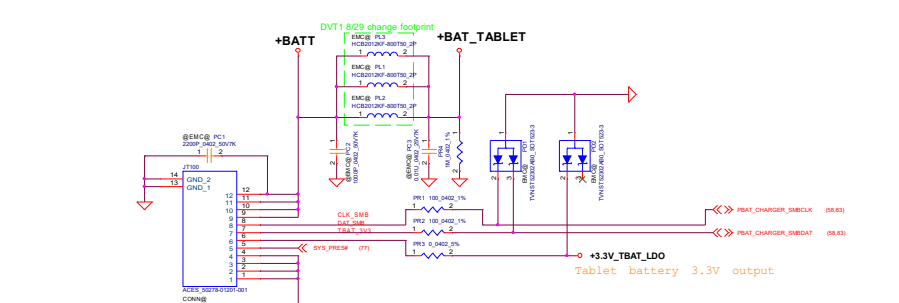
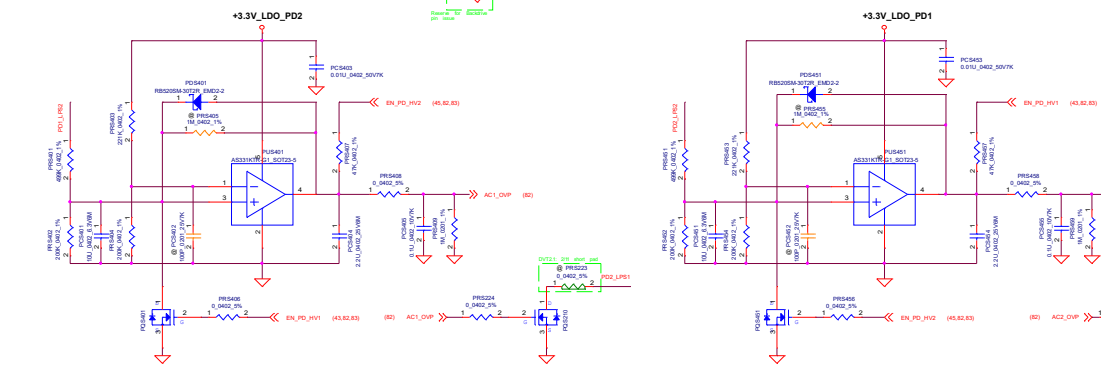
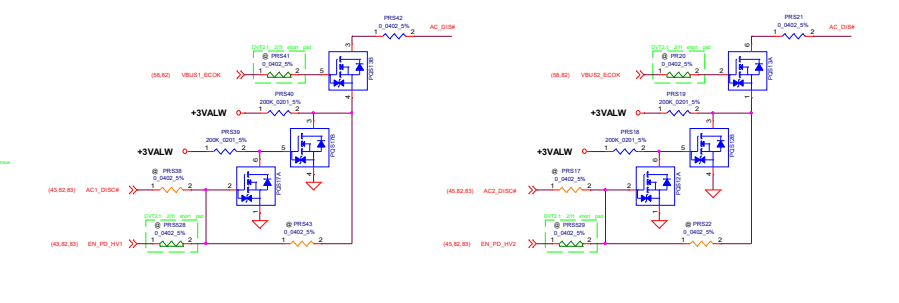
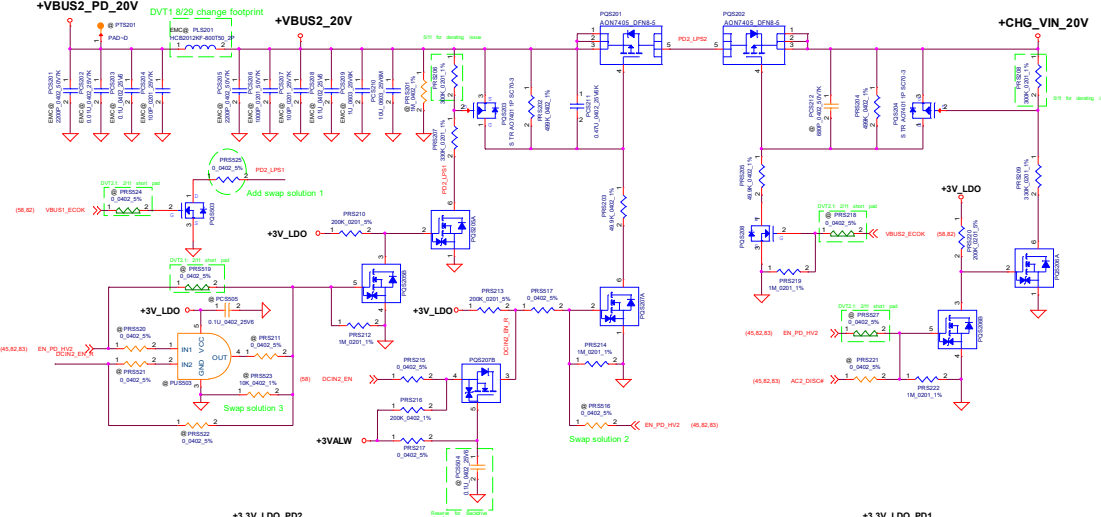


Function feild :
Rest of support elements (37.1), EMC Part(47.1)

Type C adapter input_1

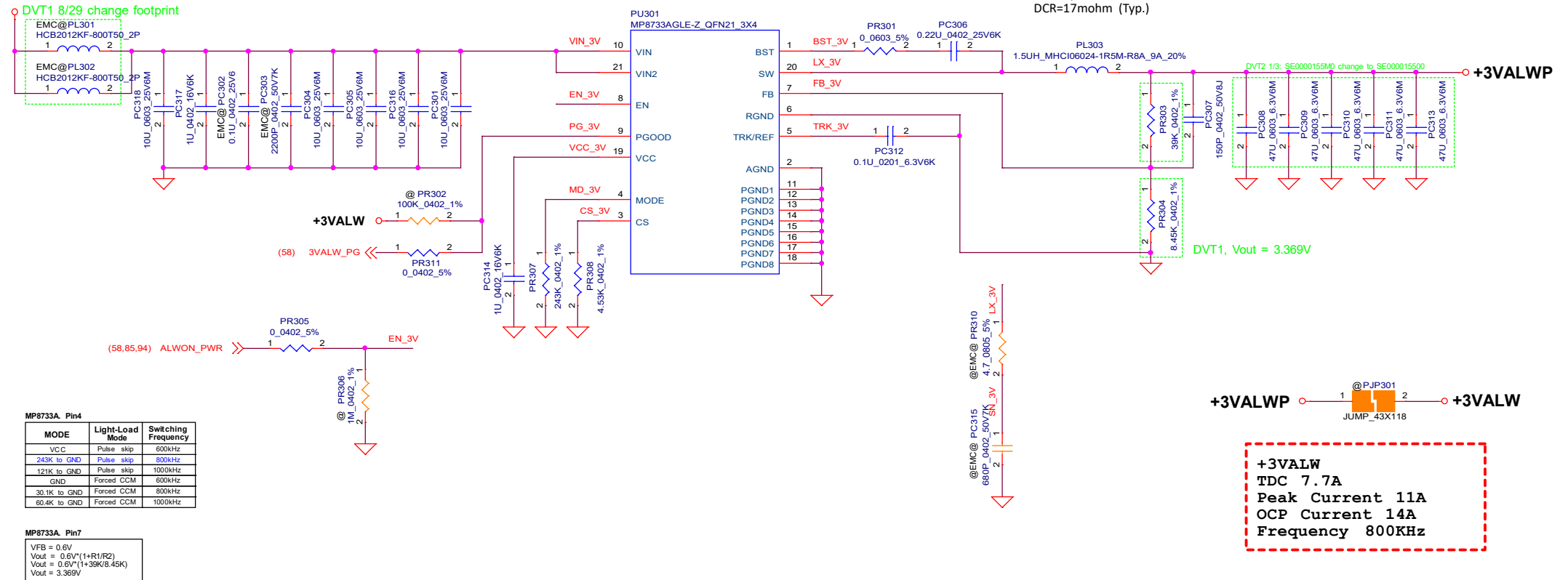


Type C adapter input_2



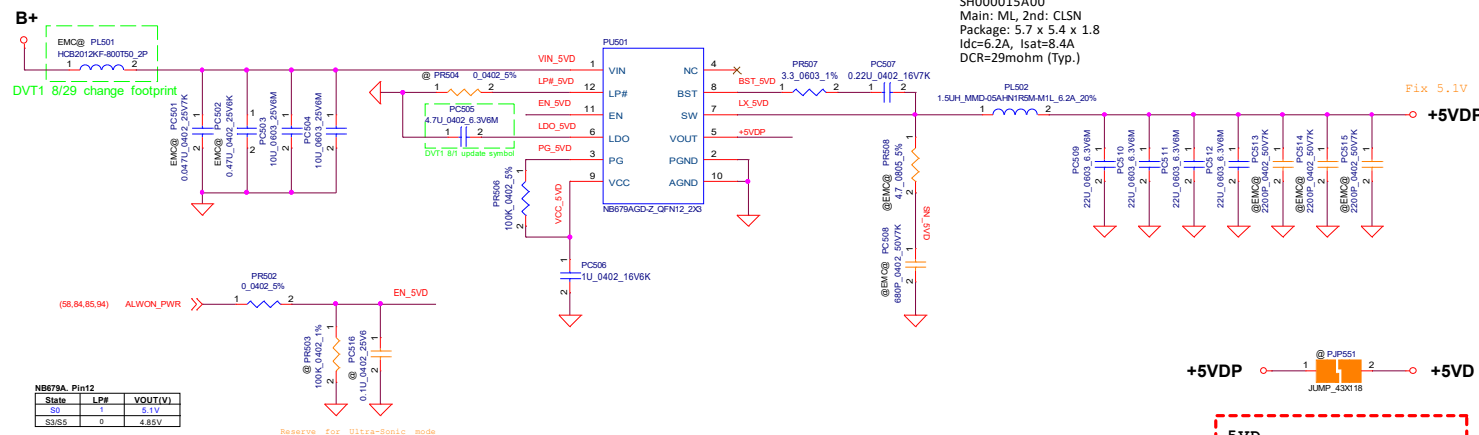
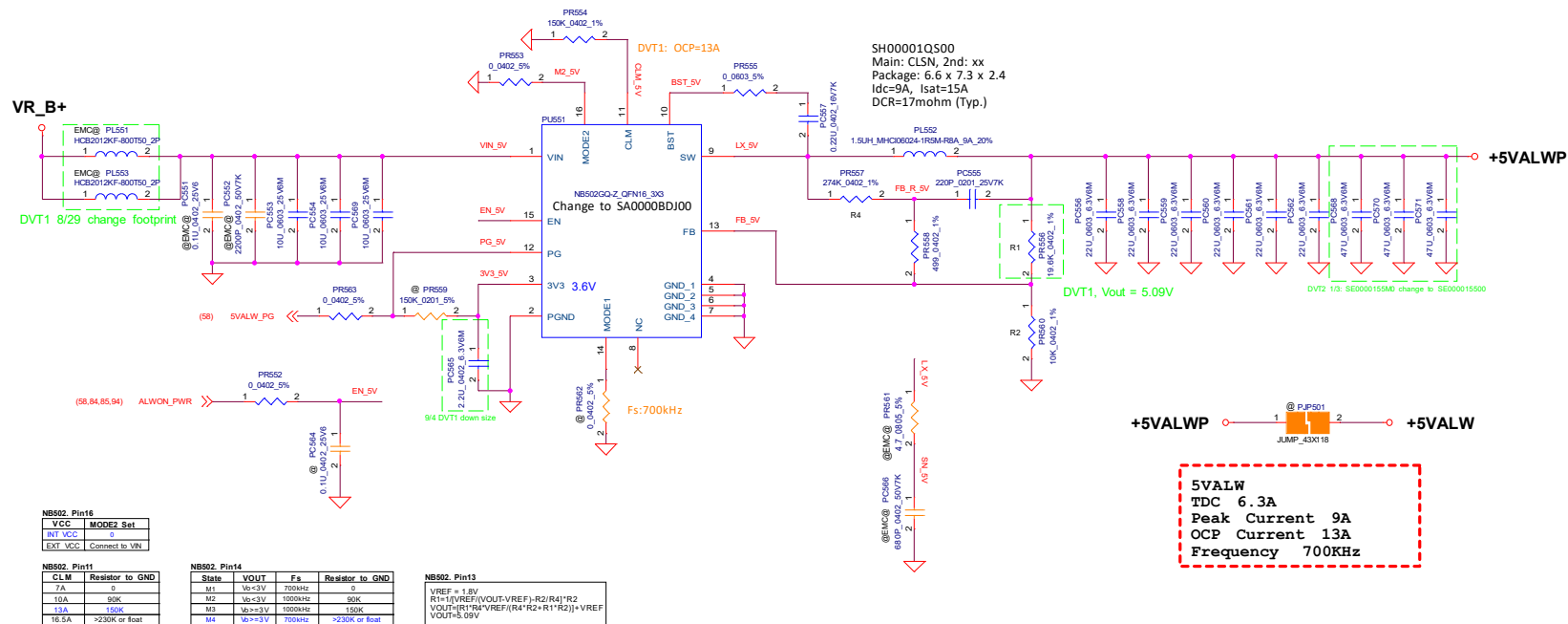
+3VALW controller(35.1), Support component(35.2)

B+

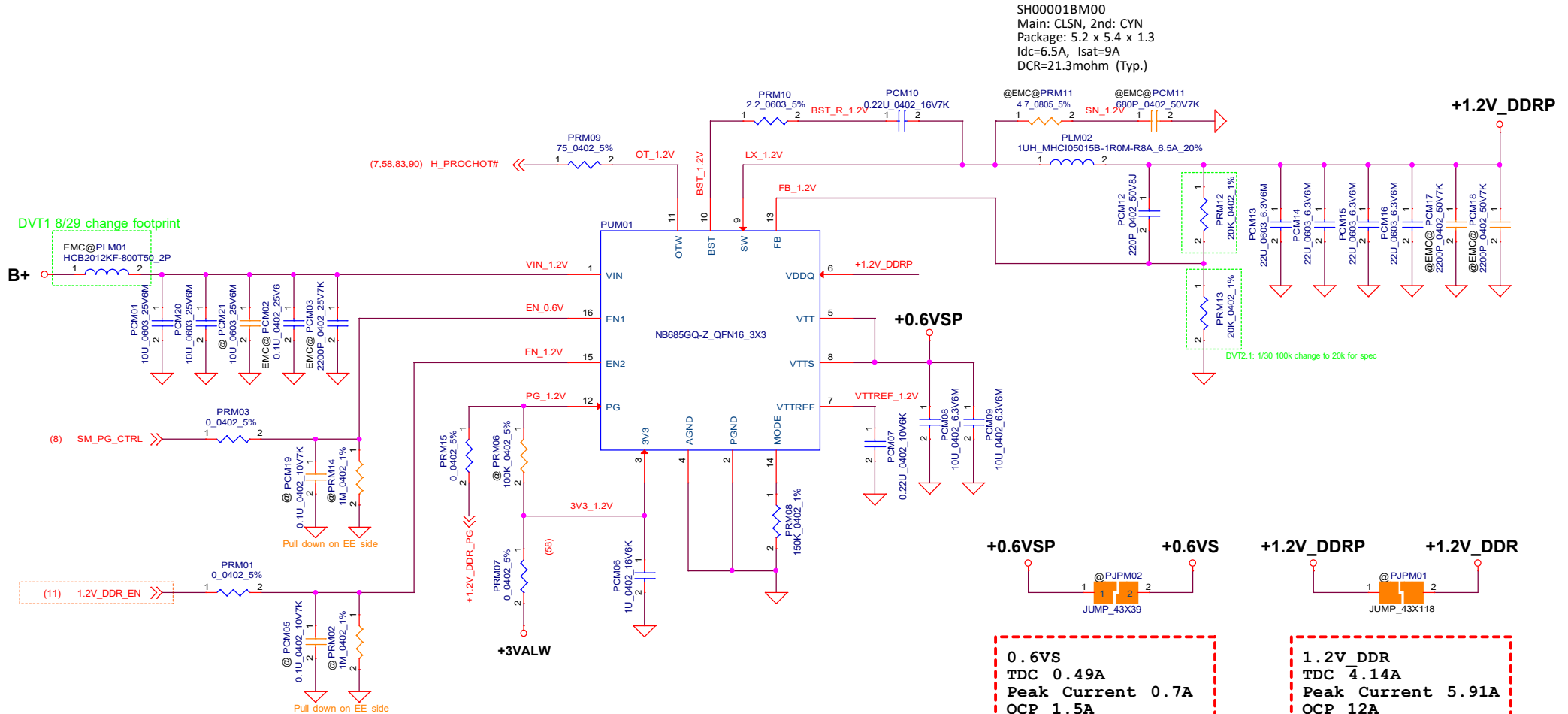


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Size		Document Number	LA-G661P	Rev	1.0
Date:		Friday, February 15, 2019	Sheet	84	of 100

+5VALW/+5VD controller(35.1), Support component(35.2)



+1.2V_DDR controller(35.3), Support component(35.4)



NB685_Pin15/16

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	H	H	ON	ON	ON
S3	L	H	ON	ON	OFF(High-Z)
S4/S5	L	L	OFF	OFF	OFF
Others	H	L	OFF	OFF	OFF

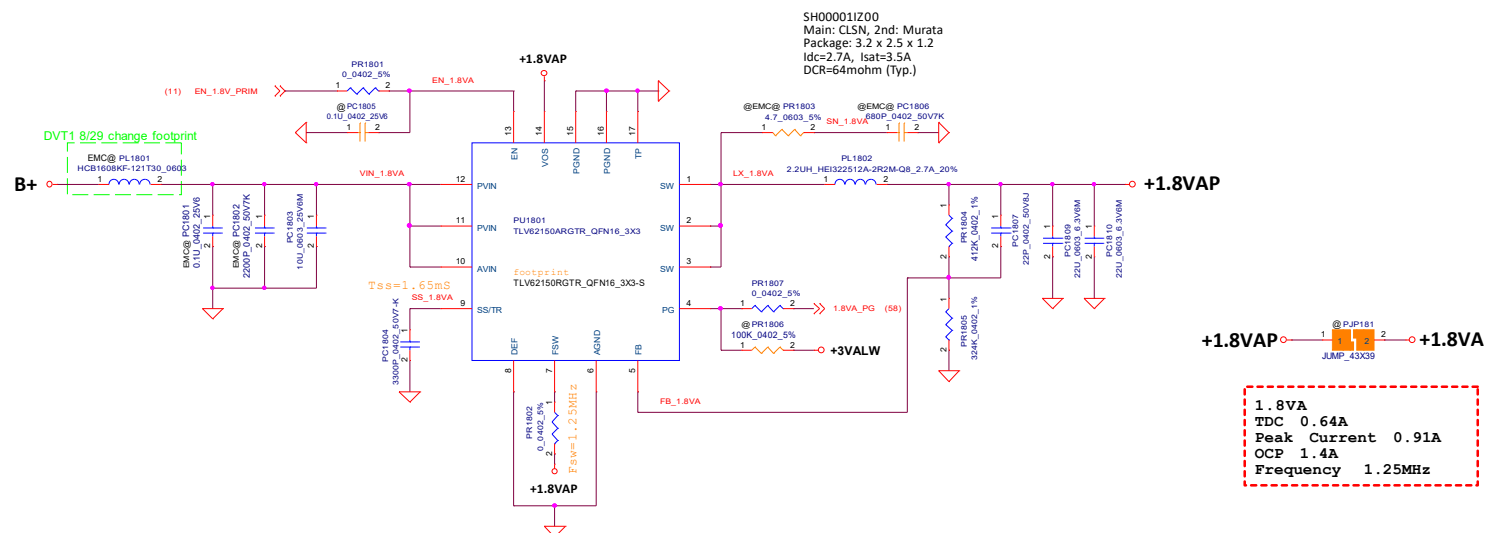
NB685_Pin14

State	USM	Fs	Resistor to GND
M1	N	700k	0
M2	Y	700k	100k
M3	N	500k	150k
M4	Y	500k	>200k

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				Date:	Friday, February 15, 2019
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				Rev	1.0

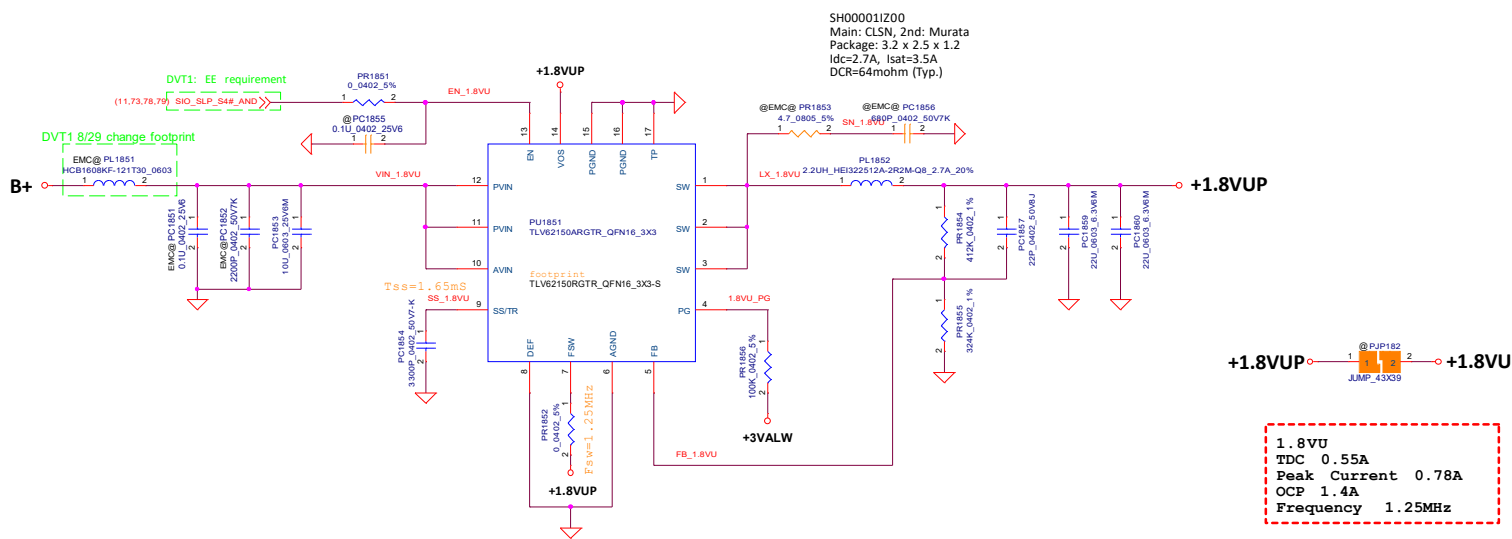
Module Design

+1.8VS controller(35.13), Support component(35.14)



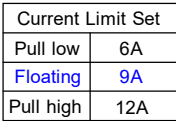
Module Design

+1.8VU controller(35.13), Support component(35.14)



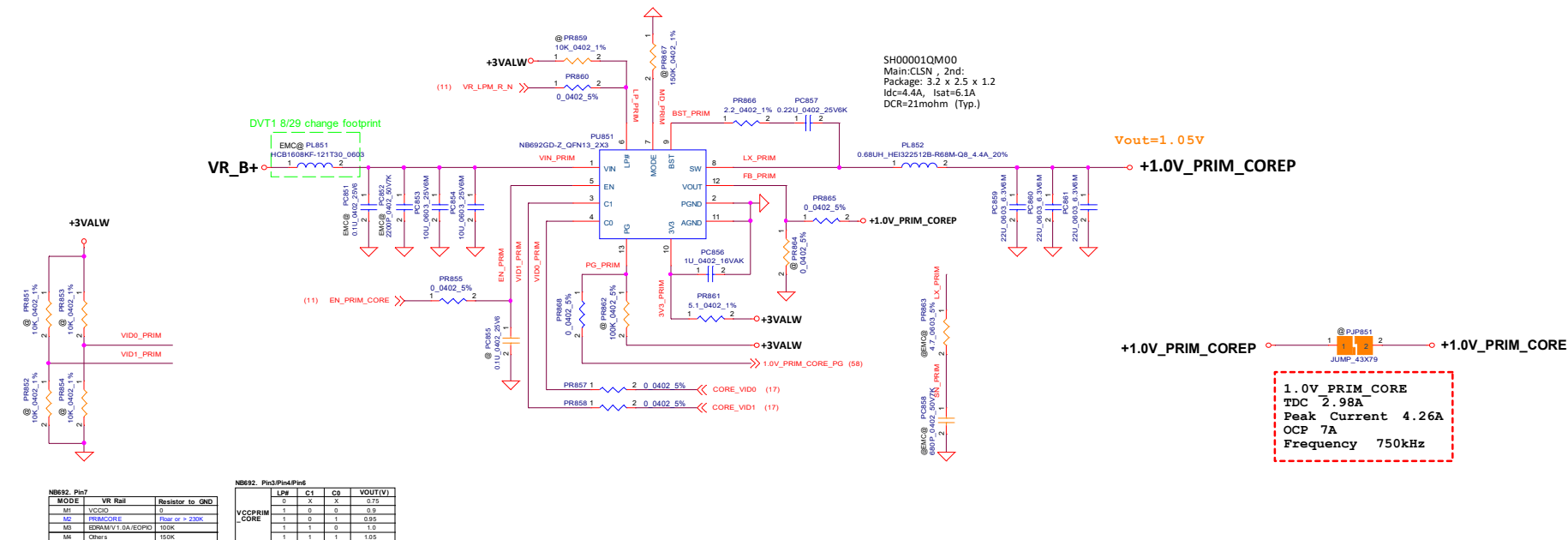
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+1.0VA controller(35.5), Support component(35.6)

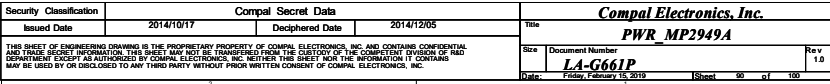


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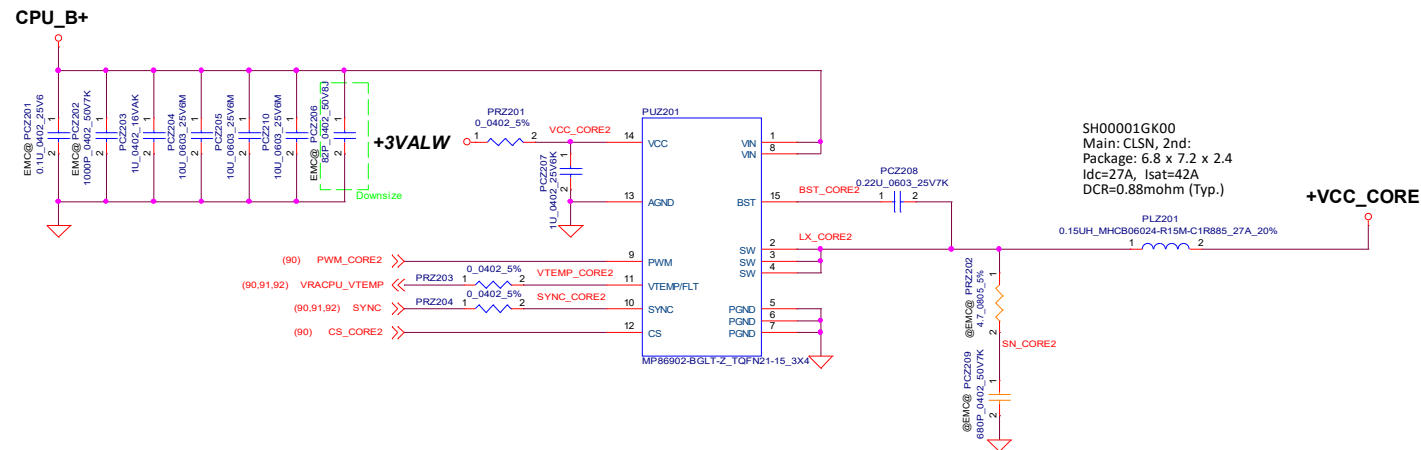
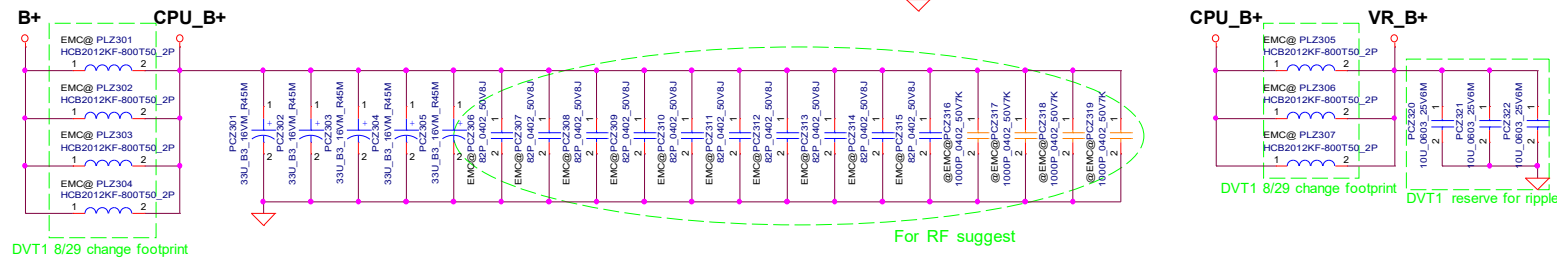
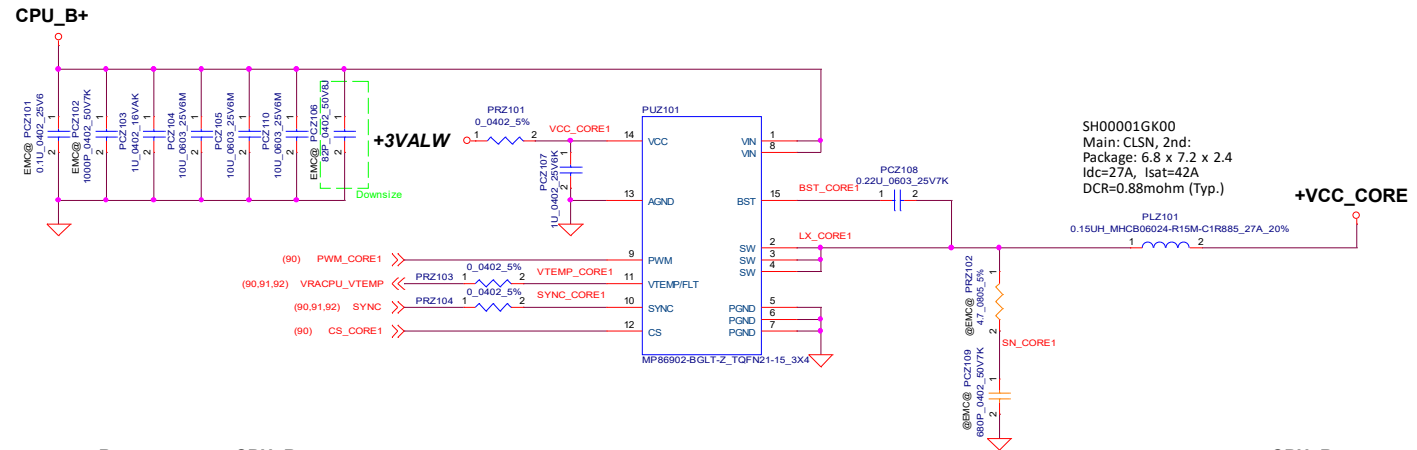
+1.0V_PRIM_CORE controller(35.39), Support component(35.40)



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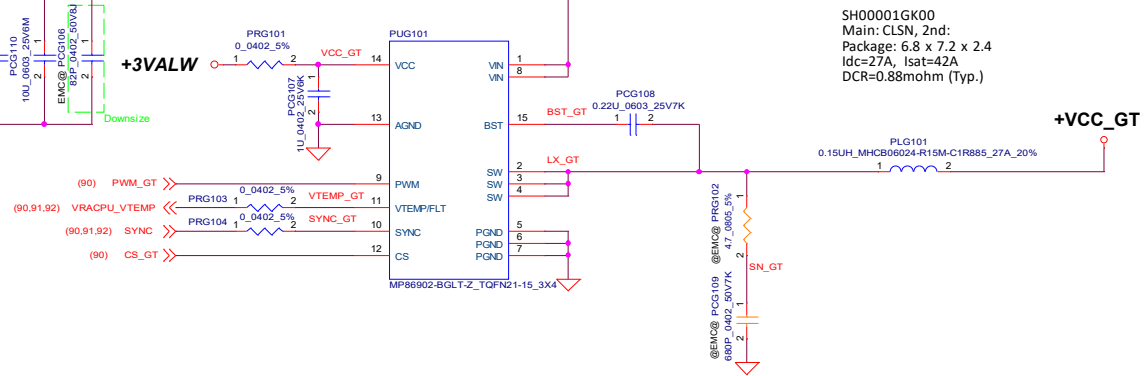
VCC_CORE Dr. MOS (36.2), Support component(36.3)



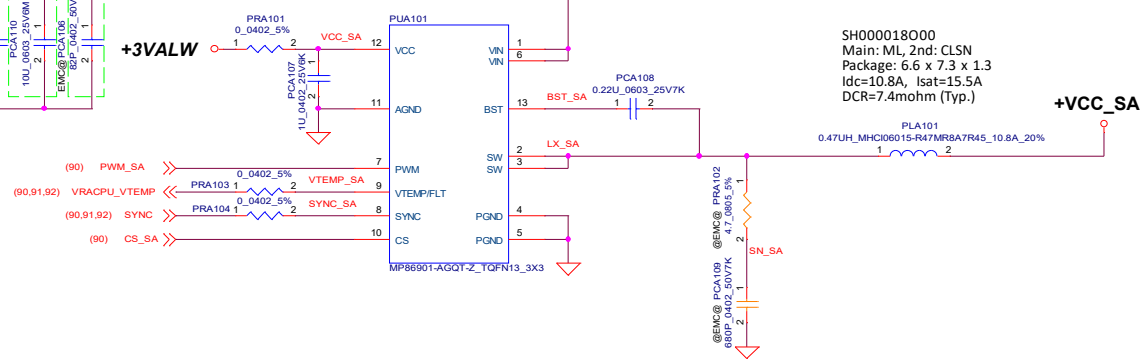
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VCC_GT/SA Dr. MOS (36.2), Support component(36.3)

CPU_B+



CPU_B+



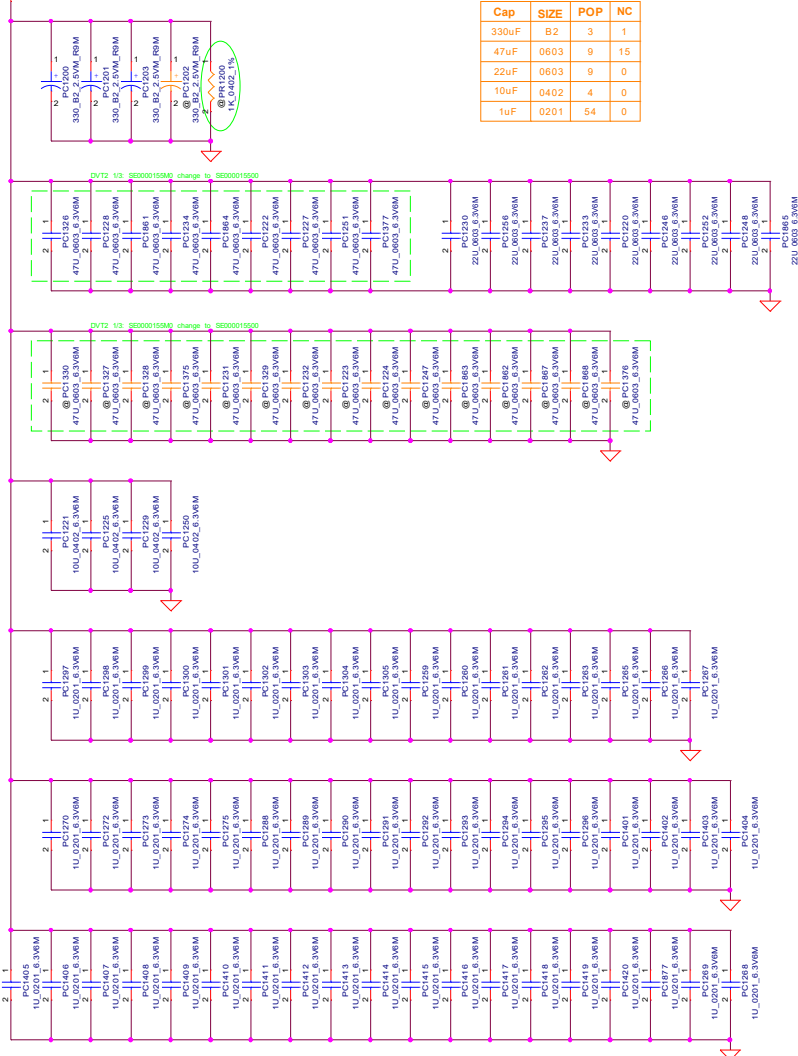
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VCC_CORE output cap(36.4), VCC_GT output cap(36.5), VCC_SA output cap(36.6)

+VCC_CORE

+VCC_CORE

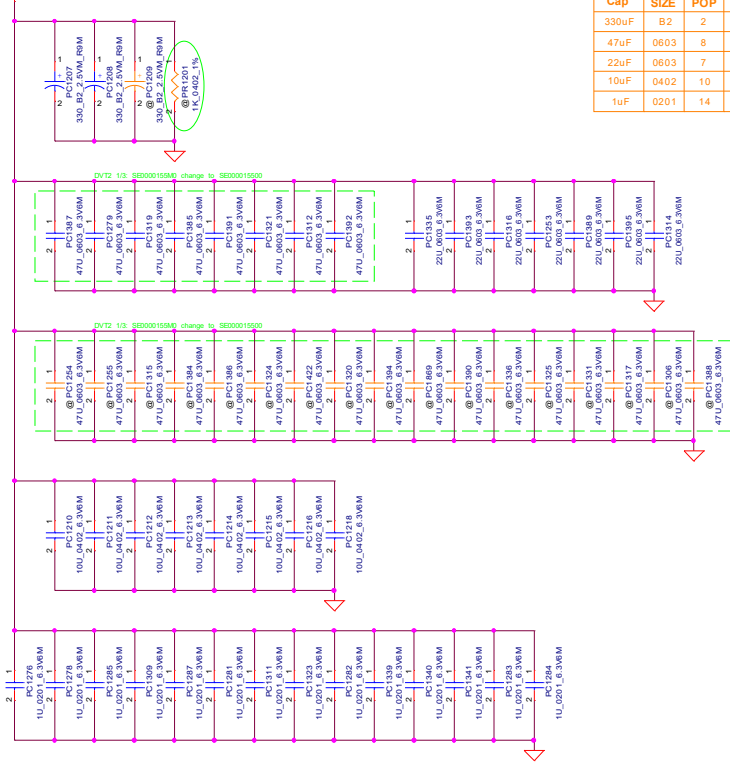
Cap	SIZE	POP	NC
330uF	B2	3	1
47uF	0603	9	15
22uF	0603	9	0
10uF	0402	4	0
1uF	0201	54	0



+VCC_GT

+VCC_GT

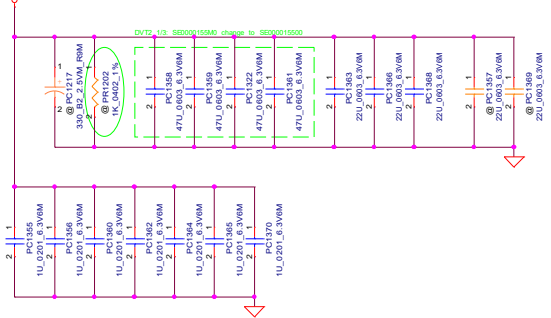
Cap	SIZE	POP	NC
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47uF	0603	8	17
22uF	0603	7	0
10uF	0402	10	0
1uF	0201	14	0



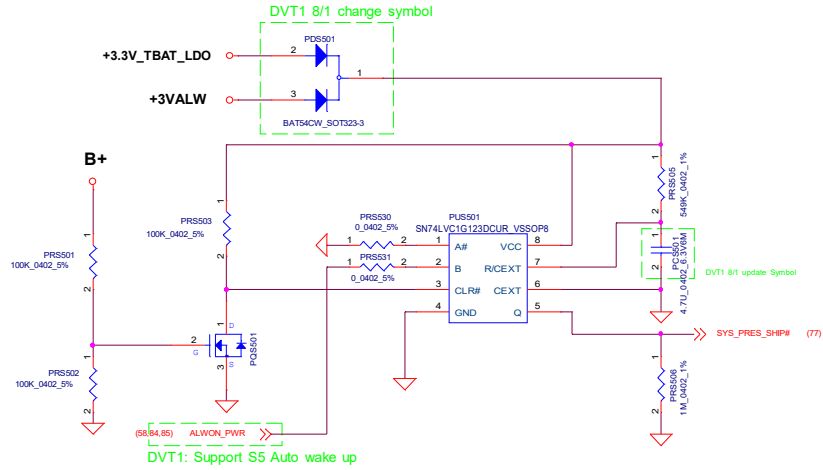
+VCC_SA

+VCC_SA

Cap	SIZE	POP	NC
330uF	B2	0	1
47uF	0603	4	0
22uF	0603	3	2
1uF	0201	7	0



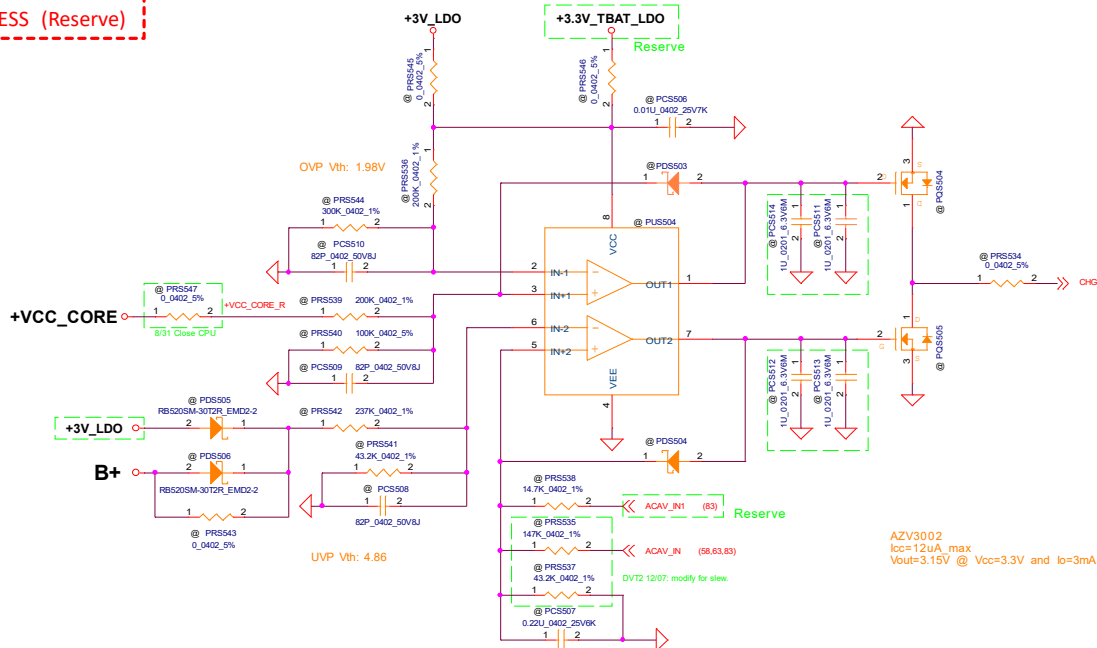
Storage mode wake up circuit



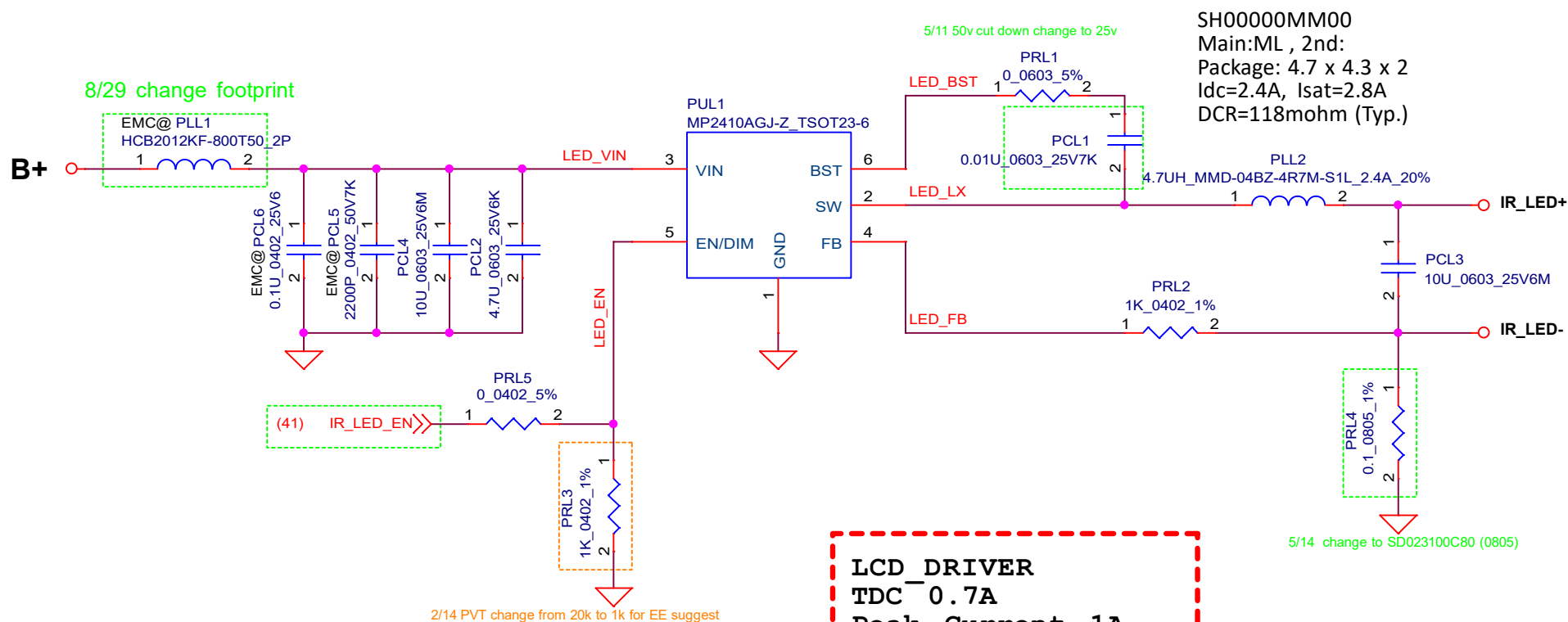
FUNCTION TABLE

INPUTS			OUTPUTS Q
CLR	\bar{A}	B	
L	X	X	L
X	H	X	L ⁽¹⁾
X	X	L	L ⁽¹⁾
H	L	↑	
H	↓	H	
↑	L	H	

SMOKELESS (Reserve)



LED driver controller(42.1), Support component(42.2)



LCD_DRIVER
TDC_0.7A
Peak Current 1A
OCP 3.6A
Frequency 1MHz

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A		B		C		D		E	
1									
2									
3									
4									

5	4	3	2	1																																			
D				D																																			
C				C																																			
B				B																																			
A				A																																			
<table><tr><td colspan="2">Security Classification</td><td colspan="2">Compal Secret Data</td><td>Compal Electronics, Inc.</td></tr><tr><td>Issued Date</td><td>2011/06/02</td><td>Deciphered Date</td><td>2013/10/28</td><td>Title</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>Size</td></tr><tr><td colspan="4"></td><td>Document Number</td></tr><tr><td colspan="4"></td><td>Rev</td></tr><tr><td colspan="4"></td><td>1.0</td></tr><tr><td colspan="4">Date: Friday, February 15, 2019</td><td>Sheet 97 of 100</td></tr></table>					Security Classification		Compal Secret Data		Compal Electronics, Inc.	Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size					Document Number					Rev					1.0	Date: Friday, February 15, 2019				Sheet 97 of 100
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				PWR-Reserve		
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